M224XAS

Disk Drives
Customer Engineering Manual

FUJITSU

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CHAPTER 1
GENERAL DESCRIPTION

1.1 General Description

1.1.1 General description

The M2241AS/M2242AS/M2243AS disk drives (called M224XAS hereafter) are compact (mini-floppy size), inexpensive, and highly reliable fixed disk drives for random access file in small computers, word processors, and terminals.

The storage capacities (unformatted) of M2241AS, M2242AS and M2243AS are 31.41MB, 54.97MB and 86.39MB respectively.

1.1.2 Features

(1) Compact size

Since the disks are 130 mm (5.12 in) in outer diameter and are driven by a DC motor directly connected to the spindle, the unit is extremely compact in size:
146 mm (5.7 in) (width) x 83 mm (3.3 in) (height) x 203 mm (8.0 in) (depth)

(2) High speed positioning

High speed head positioning is made possible by utilizing a rotary voice coil motor.

(3) High reliability

High reliability is achieved through the following features.

a. **The completely sealed disk enclosure contains a breather filter and a recirculation filter to provide a contamination-free environment.**

b. Whitney-type contact start-stop heads eliminate moving parts associated with head loading and unloading.

c. All models use LSI circuit logic and a microprocessor.

d. Head IC's are located on the head arms to amplify the small signal, reducing read errors by increasing the signal to noise ratio.

(4) Preventive maintenance

Preventive maintenance is not necessary.

(5) DC power

The direct-drive DC spindle motor requires no adjustment for line frequencies (50 Hz/60 Hz) or input power voltages (100, 115, 220 or 240 V).

(6) 5.25 mini floppy disk drive size compatibility

Because its physical size is the same as that of a mini floppy disk drive, this unit can replace a mini floppy disk drive without locker redesign.

(7) Vertical or Horizontal installation

The unit may be installed in its locker either vertically or horizontally.

(8) Low power consumption

The power consumption is 30W. This low power consumption enables the unit to be used in a wide environmental temperature range (5 to 45° C) without a cooling fan.

(9) Low noise

The unit's low noise output, approx. 45 dB (A-scale weighting) even during seeking, makes it ideal for office use.

(10) Low vibration

The unit has four rubber vibration isolators, which minimize the transfer of motion.

(11) LSIs and microprocessor

LSIs and microprocessor are used on the main printed circuit board to achieve high reliability.

1.2 Specifications

1.2.1 Performance

Specification \ Model		M2241AS	M2242AS	M2243AS
Total storage capacity				
Unformatted	(MB)	31.41	54.97	86.39
Formatted(*)		24.70	43.23	67.94
Storage capacity/track				
Unformatted	(B)		10416	
Formatted(*)	(B)		8192	
Number of disks		3	4	6
Number of heads (R/W)		4	7	11
Number of cylinders		754	754	754
Number of tracks/cylinder		4	7	11
Number of sectors			32	
Recording density	(BPI)		10200	
Track density	(TPI)		760	
Transfer rate	(KB/S)		625	
Rotational speed	(rpm)		3600 ± 1%	
Average latency time	(ms)		8.3	
Recording method			MFM	
Positioning time	Min (ms)		8	
REFER TO NOTE	Ave (ms)		33	
	Max (ms)		60	
Input voltage (Typical)			+12V±5%, 1.8A (max. 4.3A)	
			+5V±5%, 1.6A	
Maximum ripple	mV		< 100 (P-P)	
External size				
Width × height × depth	(mm)		146 × 83 × 203 (w/o panel dimension)	
Disk size	(mm)		Outer diameter 130, Inner diameter 40	
Weight	(kg)		3.0	

(*) 512 bytes/sector for 16 sectors.
256 bytes/sector for 32 sectors.

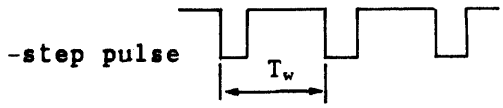
NOTE:
The M224XAS drives were designed to begin seeking after all step pulses were received (labeled Full-buffered seek mode). When the step pulse period was relatively long (e.g. >30 us), the time to Seek Complete exceeded the drive's specified access time. For example, with a period of 40 us, a maximum seek required:

(40 us x 753 tracks)	+	60 ms	=	90.12 ms
time to receive all step pulses		drive access time		actual seek time

For this reason, the circuit was redesigned to allow the drive to begin seeking without waiting for the last step pulse (labeled semi-buffered seek mode).

APPLICATION CONDITION:

1. Step pulse period $T_w \geq 20$ us
2. Key 8 of SWI should be turned "ON"



NOTES

a. If Key 8 is set "OFF", the drive is programmed for Full-buffered Mode.

b. If Key 8 is set to "ON", and the step period is shorter than 20 us, the normal seek operation cannot be performed.

c. When the drive receives more than 753 step pulses an RTZ or recalibration is performed. In the semi-buffered Mode, however, the following procedure is recommended for RTZ.

1. Set Direction false.
2. Send one step pulse.
3. Wait for seek Complete to become active.
4. Continue 2 & 3 until Track 0 become active.

EFFECT OF SEMI-BUFFERED SEEK MODE:

The relationship between step pulse period and access time in Full buffered and Semi-buffered Seek Modes are shown in Figure 1.

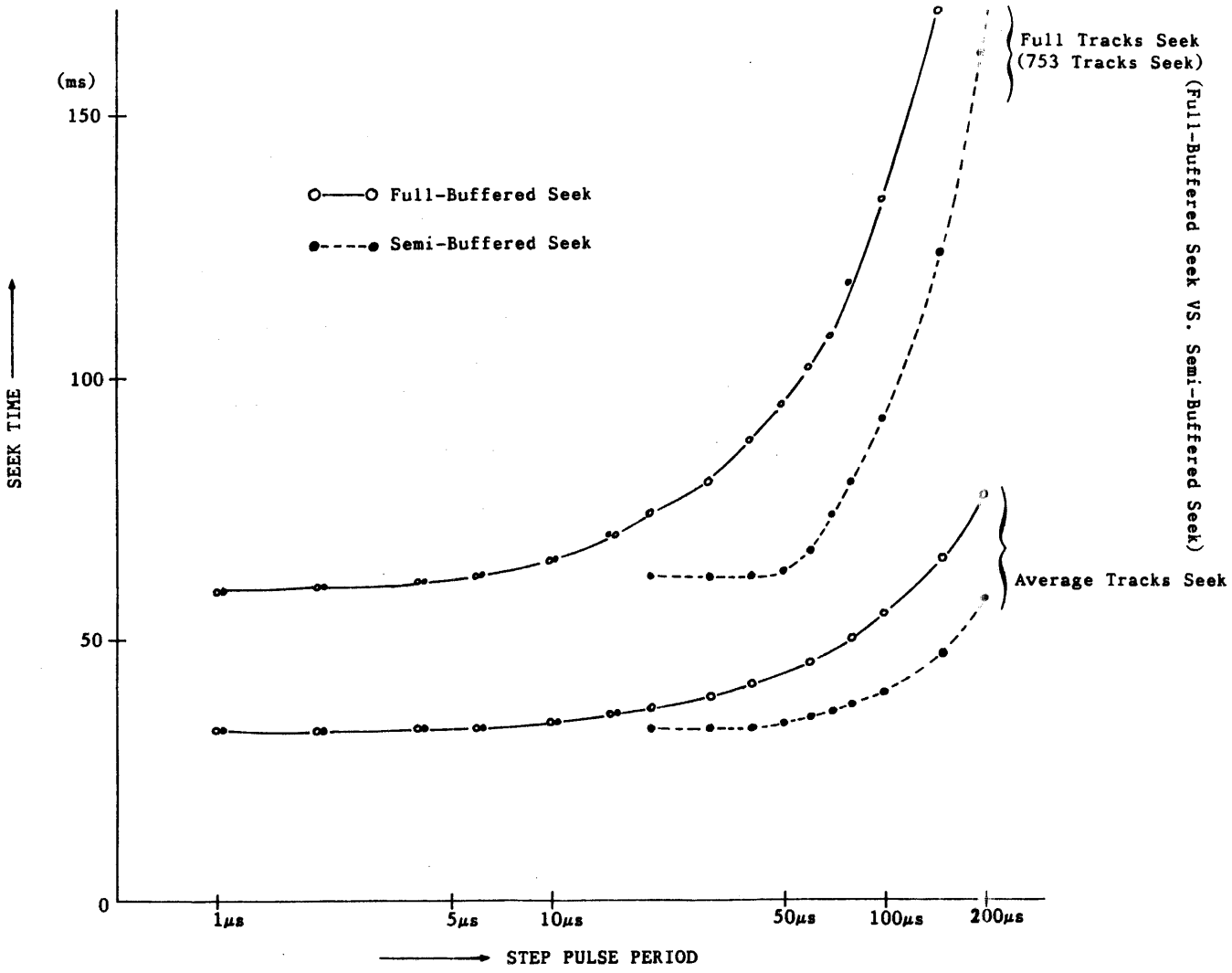
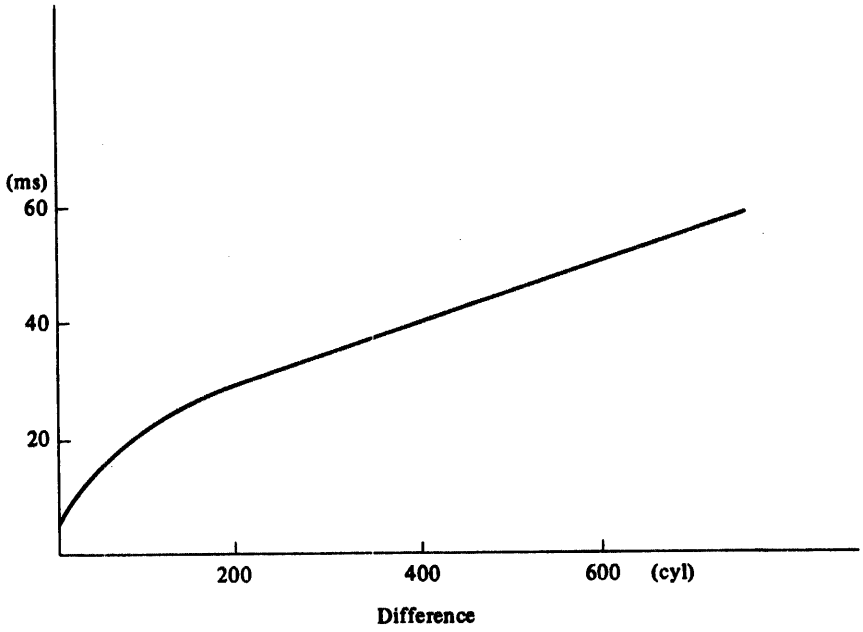


Fig. 1 ACCESS TIME CURVE

1.2.2 Seek Profile



1.2.3 Start and stop time

Start time (time from power turn on, until the unit is ready) is 20 seconds or less and stop time (time to completely stop when power is turned off) is 15 seconds or less using dynamic braking.

1.2.4 Environmental conditions

Temperature	Operating	5°C to 45°C
	Non-operating	-40°C to 60°C
	Gradient	15°C/h or less
Relative humidity	Operating	20% to 80% RH
	Non-operating	5% to 95% RH (Moisture must not condense.)
Vibration	Operating	Less than 0.2G (3 to 100 Hz) 2 min x 30 cycles (except resonance point) (sinusoidal waveform)
	Non-operating (power-off state after installation)	Less than 0.4G (3 to 100 Hz) 2 min x 30 cycles (sinusoidal waveform)
Shock	Operating	Less than 2G (maximum 10ms)
	Non-operating	Less than 20G (maximum 10ms)
Altitude above sea level	Operating	3,000m or below
	Non-operating time	12,000m or below

1.2.5 Power supply requirements

(1) Input voltage and permissible input voltage variation

	Input voltage
+12 V	+12 V±5%
+5 V	+5 V±5%

The above values are voltages at the power supply input connector of the unit.

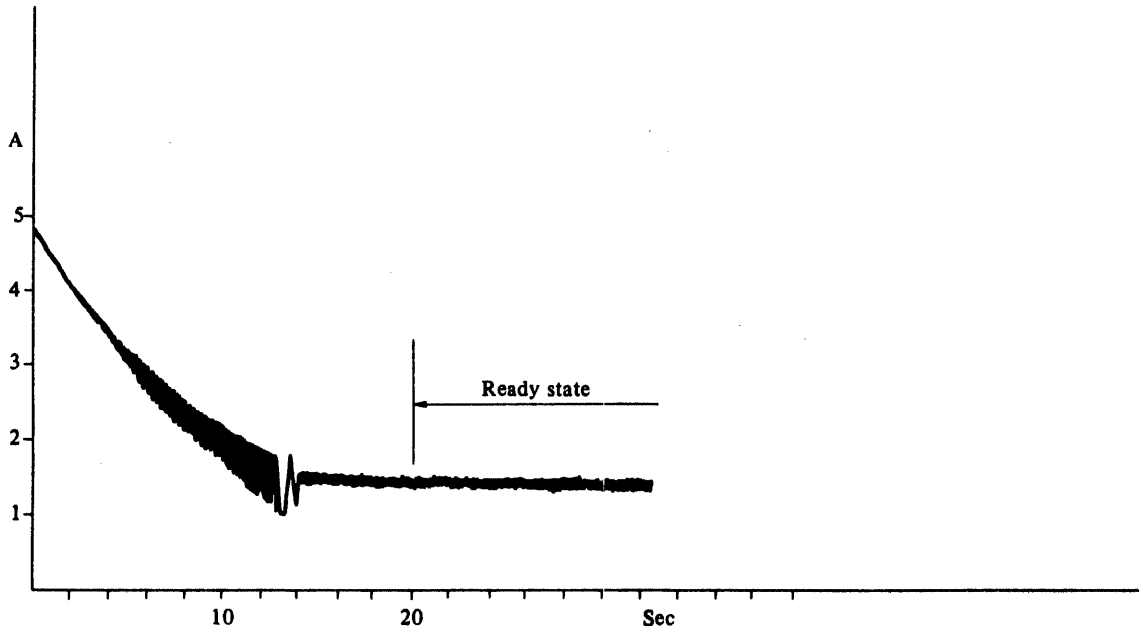
(2) Power supply requirements (minimum)

Voltage	Power-On	Seeking	Idle
+5	2.2A	2.0A	1.6A
+12	4.3A	3.1A	1.8A

Figure 1.1 shows current waveforms of +12V power during the following conditions:

- Spindle motor begins to rotate
- During seek operation

(i) Spindle motor begins rotation



(ii) Alternate Seeking and reading 0 to 227 cylinders

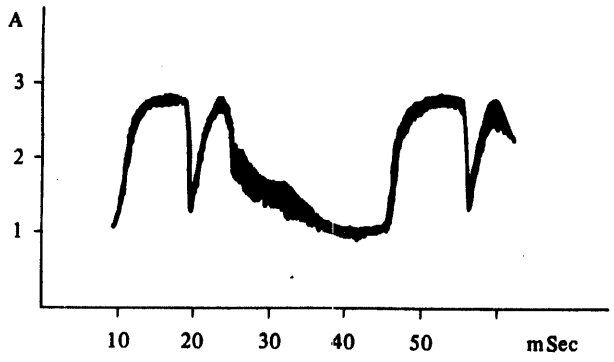


Figure 1.1 Current waveform of +12V power

1.2.6 Reliability

(1) Mean Time Between Failures (MTBF)
M224XAS has a design MTBF of more than 20,000 hours. (After an initial 3-month period.)

Note: The MTBF is defined as follows:
MTBF = Operating Time (hours)/The number of Equipment Failures from All Field Sites.

Operating time is total power on time.

Failure of the equipment means failure that requires either repairs, adjustments, or replacement. Mishandling by the operator, failures due to bad environmental conditions, power trouble, controller trouble, cable failures, or other failures not caused by the equipment are not included.

(2) Mean Time To Repair (MTTR)
MTTR is the average time taken by a well-trained service technician to diagnose and repair a unit malfunction. The M224XAS is designed for a MTTR of 30 minutes or less.

(3) Service life
Overhaul of the M224XAS is not required for the first five years.

(4) Power loss
Integrity of the data on the disk is guaranteed against all forms of abnormal DC power failure except a power failure during writing.

1.2.7 Error rate

Errors detected upon initialization and replaced by an alternate record are not included in the error rate.

(1) Recoverable error rate
A recoverable error is one which can be read correctly within one retry and should not exceed 10 errors per 10^{11} bits read.

(2) Non-recoverable error rate
Errors that cannot be recovered within 16 retries are included in the MTBF.

(3) Positioning error rate
The rate of positioning errors recoverable by one retry is 10 errors or less per 10^{7} seeks.

(4) Media error

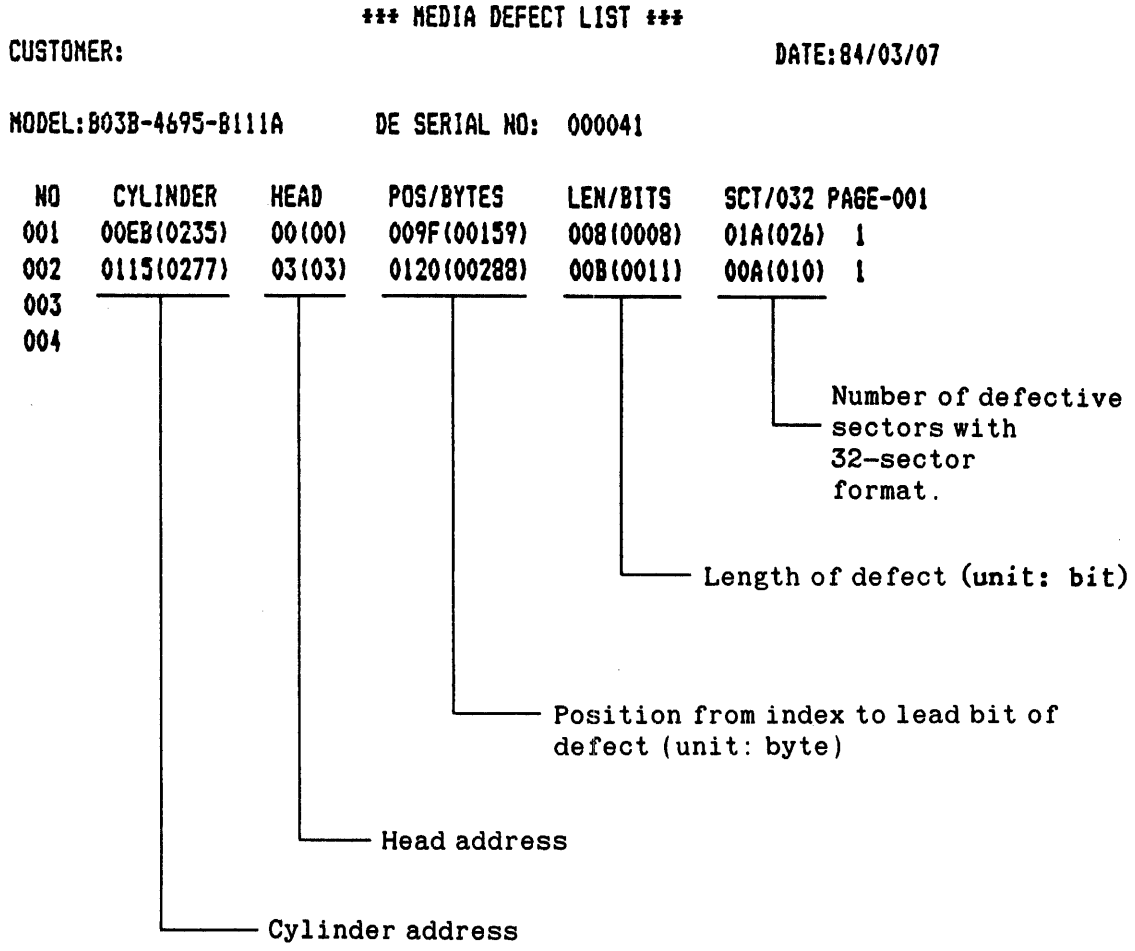
(a) All tracks of cylinder 0 are defect free.

(b) The maximum number of defects in the M224XAS are as follows:
M2241AS . . . . . 32 or less
M2242AS . . . . . 55 or less
M2243AS . . . . . 86 or less

Note: The number of defects per one surface is 24 or less
Defect length $\geq$ 64 bytes

(3) Media defect list

Media defects for units shipped from the factory are listed on the MEDIA DEFECT LIST and this list is attached to each drive. The following figure shows an example of the MEDIA DEFECT LIST. Locations are in hexadecimal; numbers in parentheses are decimal equivalents.



1.3 Structure

1.3.1 Structure of device

Figure 1.2 shows the structure of the device.

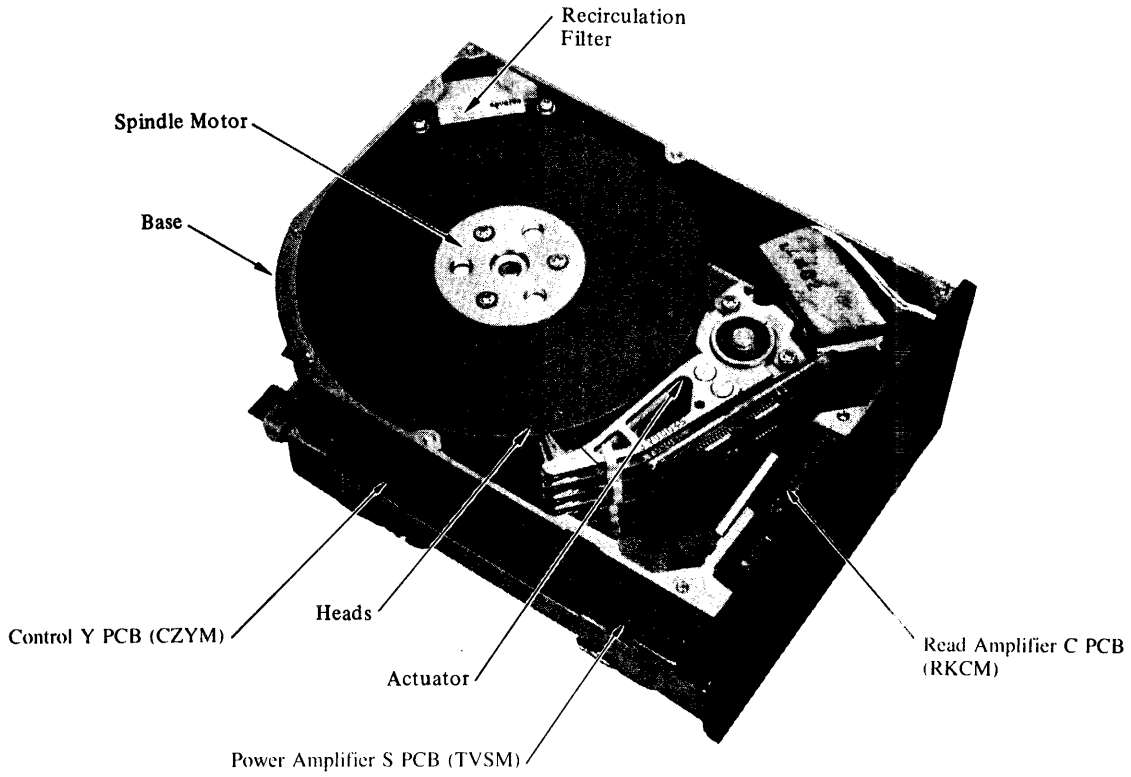


Figure 1.2 Structure

CHAPTER 2
INSTALLATION

2.1 General Description

This chapter describes unpacking, installation and cabling of the M224XAS.

2.2 Unpacking

The M224XAS is shipped in a carton with form fitting cushions. An exterior view of the carton is shown in Figure 2.1.

(1) Place the carton on a flat surface. Ensure that the top of the box, indicated by a ''This Side Up'' sign, is oriented correctly.

(2) Open the carton and take out the top cushion.

(3) Pull the M224XAS out of the carton by grasping its base. Move the drive slowly and carefully, to prevent unnecessary shock.

CAUTION

When transporting, installing or servicing, avoid shocks to the drive to protect the heads and media from damage.

When transporting the drive, use the specified carton.

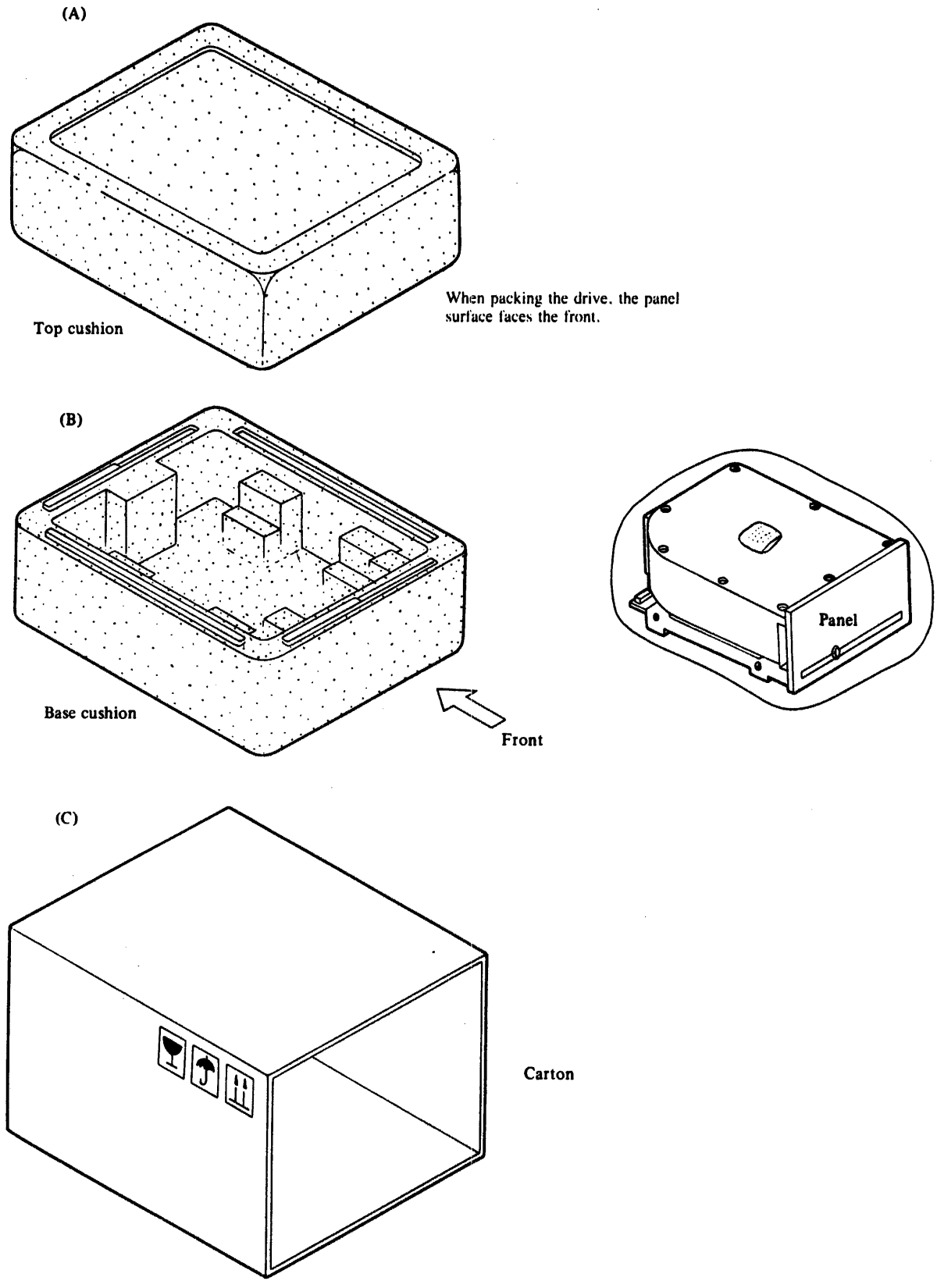


Figure 2.1 Exterior view of cartion

2.3 Visual Inspection

After unpacking, check the following:

(1) There should be no cracks, rust or other damage.

(2) All parts should be firmly fixed, there should be no loose screw, etc.

(3) The MEDIA DEFECT LIST should be attached.

2.4 Cable Connection

A total of four drives can be connected to one controller.

Cable connection is as follows.

2.4.1 Unit connectors

The A/B cable edge connectors, powers, and signal ground (SG) connectors are arrayed as shown in Figure 2.2.

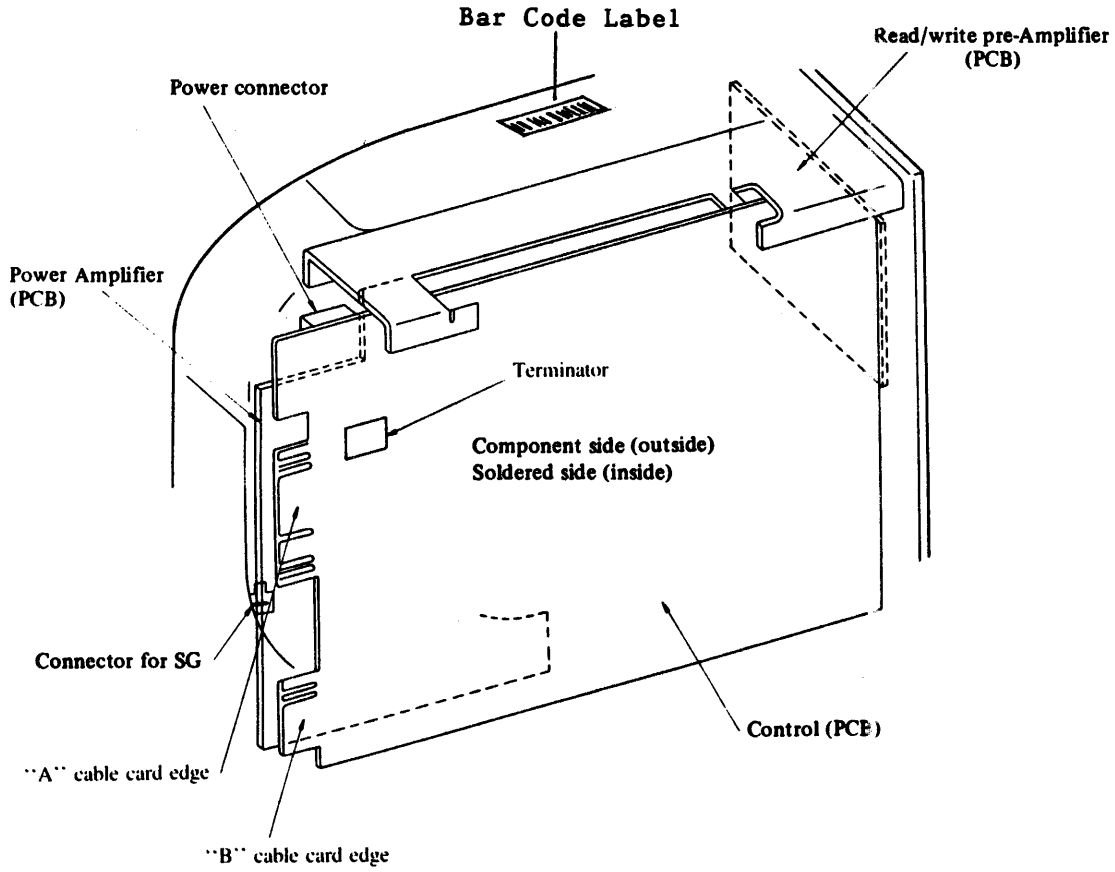


Figure 2.2 Unit Connectors

2.4.2 Connection

Connection of units to their controller is shown in Figure 2.3. To connect more than one unit, the A cable (control signals) must be connected in series and the B cables (R/W signals) in parallel. The termination of control signals must be performed only at the last drive. The termination resistor pack must be removed from all but the last drive. See Figure 2.2 for terminator location.

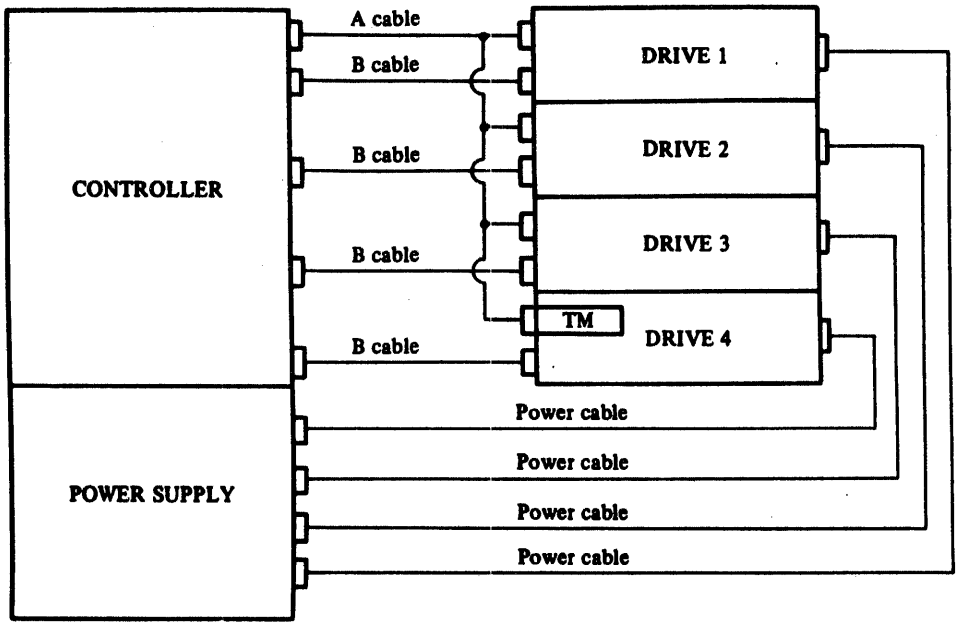


Figure 2.3 Multiple Units Connection

2.4.3 Cable connector specifications

The recommended cable connector specifications are listed in Table 2.1.

Table 2.1 Cable Connector Specifications

Connector	Name	Spec. No.	Manufacturer
Cable A (34P)	Cable connector	FCN-767J034-AU/1 or 88373-3 or 3463-0001	FUJITSU AMP 3M
	Unit card edge	—	—
	Cable	455-248-34 or 171-34	SPECTRA-STRIP ANSLEY
Cable B (20P)	Cable connector	FCN-767J020-AU/1 or 88373-6 or 3461-0001	FUJITSU AMP 3M
	Unit card edge	—	—
	Cable	455-248-20 or 171-20	SPECTRA-STRIP ANSLEY
Power cable	Cable connector	1-480424-0	AMP
	Unit connector	1-350211-1	AMP
	Contact	170121-4	AMP
	Cable	AWG 18 (+5V, RTN) AWG 18 (+12V, RTN)	—
SG cable	Fasten receptacle for cable side	62187-1	AMP
	Fasten tab for the device	61761-2	AMP
	Cable	AWG 20	

2.5 Installation

2.5.1 Device outer dimensions

Figure 2.4 shows the device outer measurements and mounting dimensions. Dimensions are in millimeters.

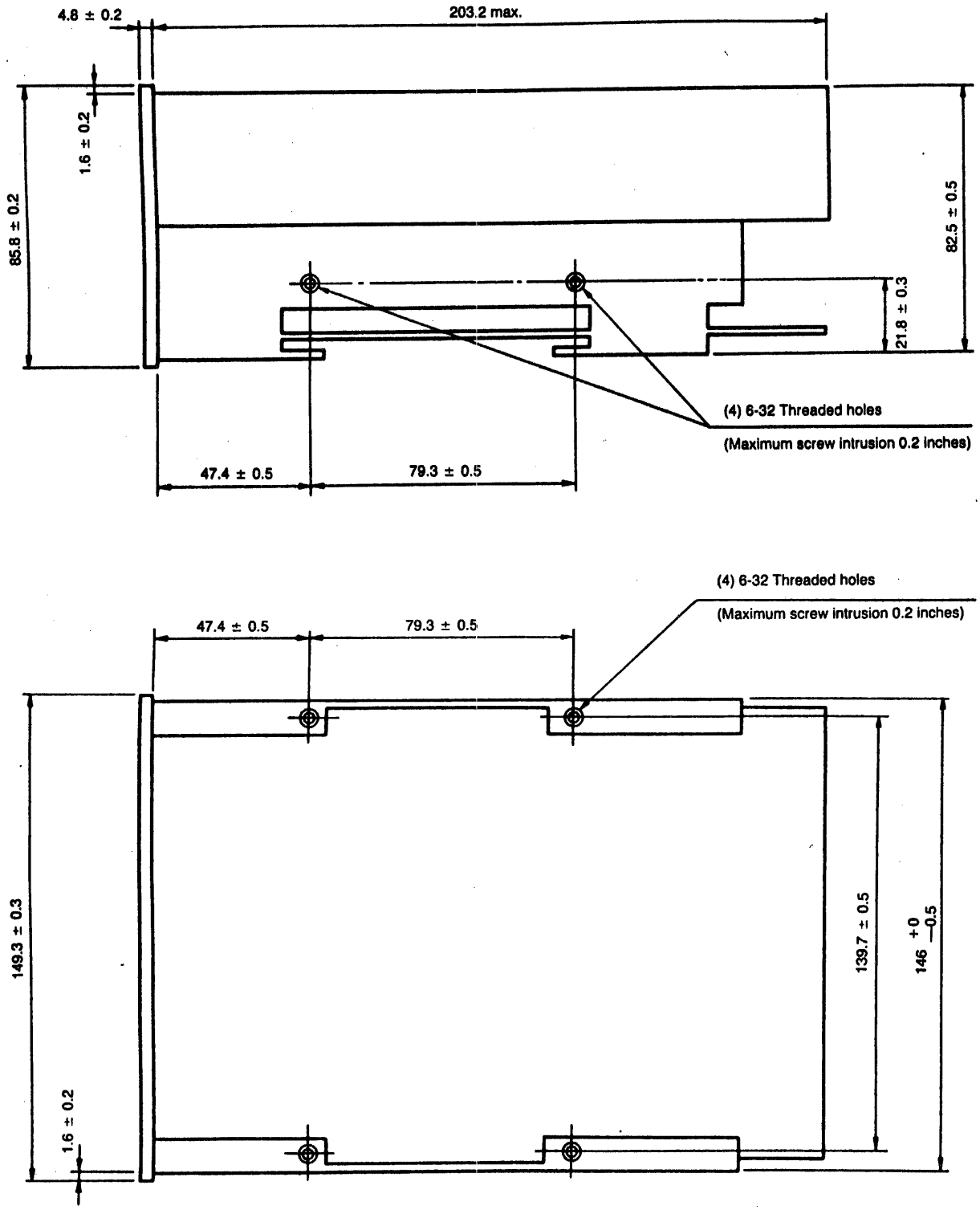
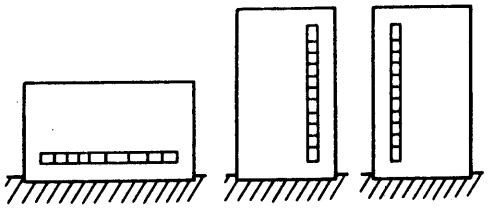


Figure 2.4 Device Outer Measurements

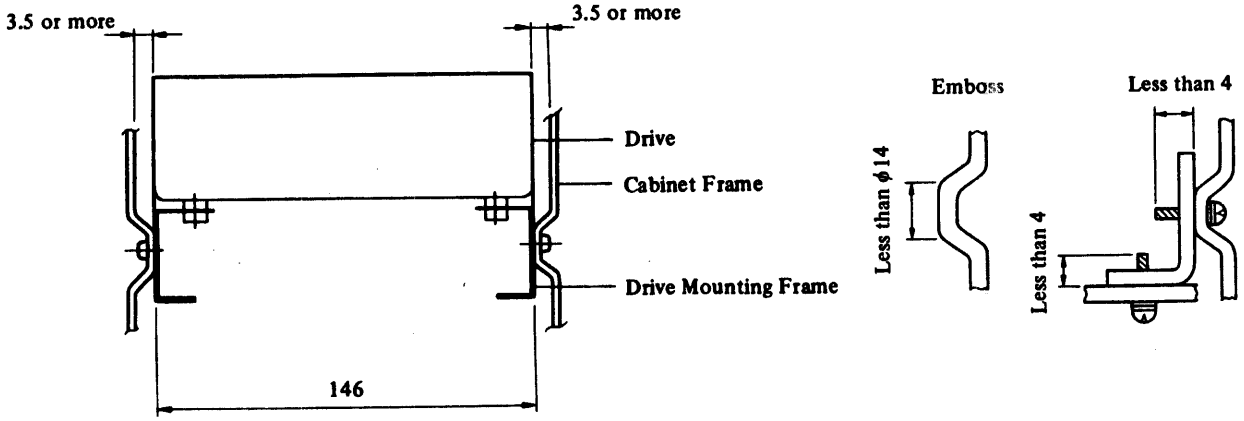
2.5.2 Notes on installation

(1) The unit may be installed horizontally or vertically as follows.

FRONT VIEW

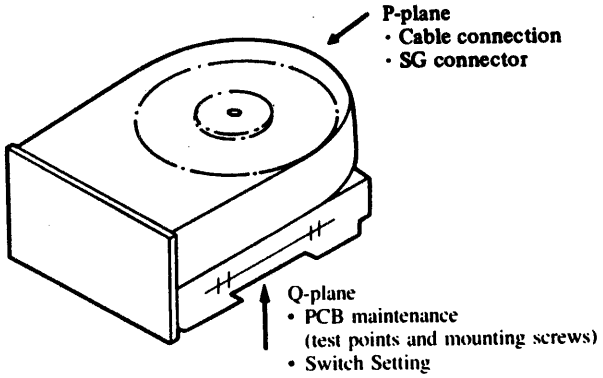


(2) Frame structure
The disk enclosure (signal ground) is isolated from the drive mounting frame (frame ground).
When mounting the drive in a cabinet frame, the frame should clear the drive by at least 3.5 mm to prevent the drive from touching the cabinet frame.



(3) Ambient temperature
The operating temperature range of the drive is specified at a distance of 3 cm from the unit.

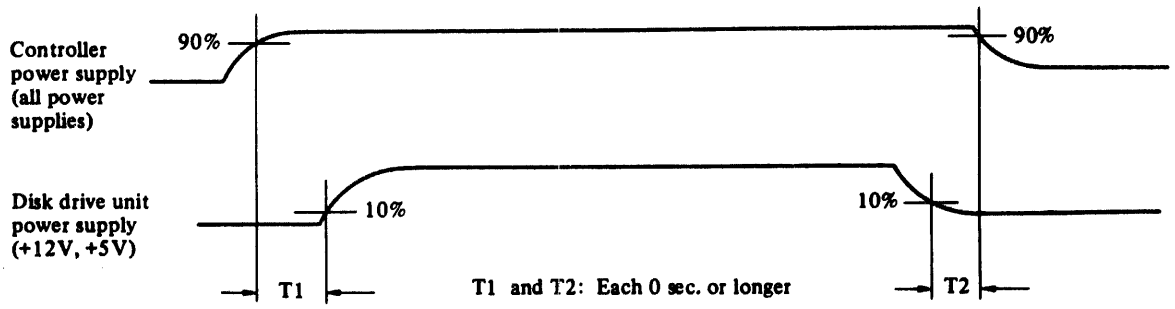
(4) Service area



2.6 Power On/Off Sequence

If the Write Gate signal from the controller is off before applying or removing power, the voltages (+12 V, +5 V) to the drive need not be sequenced. That is, recorded data will not be destroyed nor will mechanical or electric problems occur. To maintain the Write Gate signal in the off state at the time of unit power-on or -off, the basic sequence between the power supply of the controller and drive unit is as follows.

(1) Basic sequence



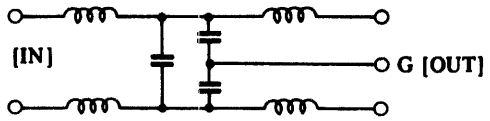
Note) The power supplies of the disk drive unit (+12 V, +5 V) need not be sequenced when above timing is observed.

(2) If the controller and the drive share a common supply and the Write Gate interface signal is determined only by +5 V, power sequencing is unnecessary. This is because the +5 V level is monitored within the drive.

2.7 Others

(1) **To eliminate AC line noise, a noise filter of the specifications given below should be incorporated in the AC input terminal of the disk drive power supply.**

Attenuation characteristic; 40 dB or greater at 10 MHz
Circuit configuration; T type shown below is recommended.



2.8 Switch setting procedure

The functions and assignment procedures of the switch are described below. The mounting location on the main PCB is illustrated in Figure 2.5.

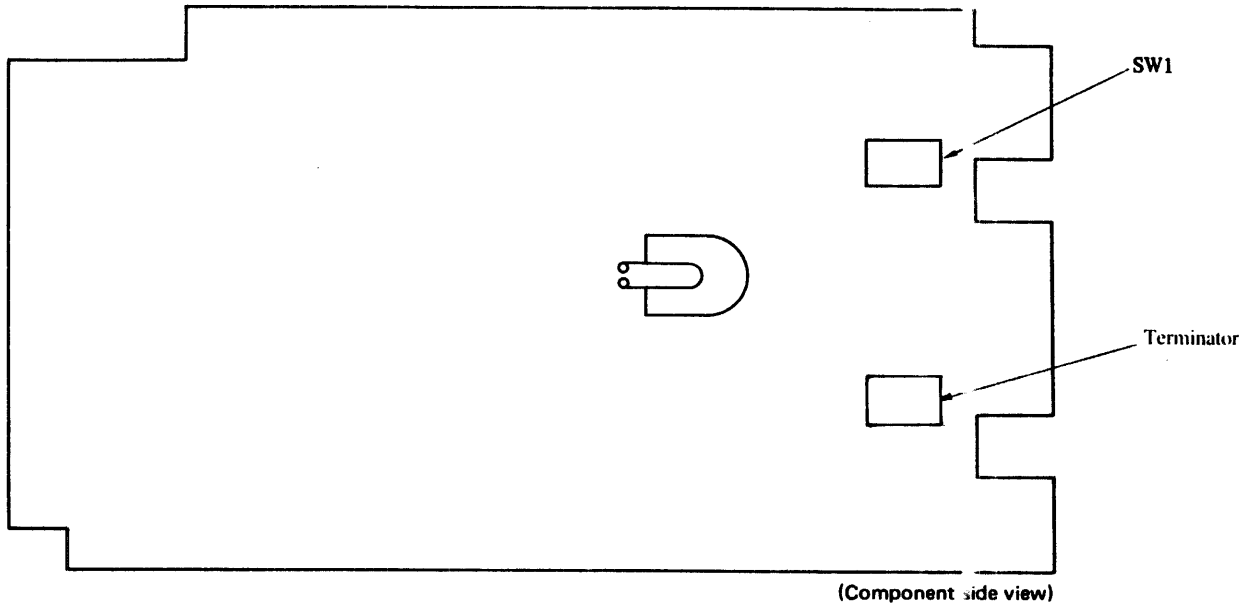


Figure 2.5 Switch Mounting Location

(1) Control of DRIVE SELECTED Signal ..... Key 5 in SW1
"ON" side ... A drive is in a selected state regardless of DRIVE SELECT 1 ∿ 4, which means DRIVE SELECTED signal is always true and all Input/Output signals are validated without selecting the drive.
"OFF" side .. DRIVE SELECTED signal is true and all Input/Output signals are validated only when a drive is selected with DRIVE SELECT 1∿4.

(2) DRIVE SELECTION ..... Key 1 ∿ Key 4 in SW1
Key 1∿4 in SW1 are used to select one of up to a maximum of four drives. The relevant one of four keys is to be turned ''ON'' while the others should be turned ''OFF.'' The selection procedures are shown in Table 2.2.

Table 2.2 Device Selection

DRIVE NUMBER	Key Number in SW1			
	1	2	3	4
1	o	×	×	×
2	×	o	×	×
3	×	×	o	×
4	×	×	×	o

o: "ON"
×: "OFF"

(3) MOTOR-ON . . . . . Key 6 and 7

When multiple drives are connected to a system, the +12V power supply may be overloaded. To prevent such a situation, a circuit was added which allows for power-up sequencing by the system.

The controller may send an enabling signal, Motor-On, over the 'B' cable (Pin 5).

The drive monitors Motor-On signal for one second after power is applied and waits for this signal to become true (low level at interface connector).

Motor-On signal can not be used to stop the spindle motor.

The function is controlled by Keys 6 and 7 of Switch 1.

Settings are as follows:

	Key 6	Key 7
Motor-On Enabled	OFF	ON
Motor-On Disabled	ON	OFF

When the Motor-On function is disabled, the spindle motor will begin rotating one second after power is applied.

This signal is not gated by Drive Select signal.

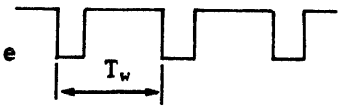
If Motor-On is enabled and Motor-On signal is not received on the interface, the drive will not start.

(4) FULL BUFFERED/SEMI-BUFFERED SEEK MODES . . . . . Key 8

The M224XAS drives were designed to begin seeking after all step pulses were received (labeled Full-buffered seek mode). When the step pulse period was relatively long (e.g. >30 us), the time to Seek Complete exceeded the drive's specified access time.
For this reason, the circuit was redesigned to allow the drive to begin seeking without waiting for the last step pulse (labeled semi-buffered seek mode).

APPLICATION CONDITION:

1. Step pulse period $T_w \geq 20$ us
2. Key 8 of SWI should be turned "ON"



NOTES

a. If Key 8 is set "OFF", the drive is programmed for Full-buffered Mode.

b. If key 8 is set "ON", and the step period is shorter than 20 us, the normal seek operation cannot be performed.

c. The drive will accept step pulses with a period between 0.3 μs and 200 μs. When the period is between 0.3 μs and 19 μs, the drive must be programmed to operate in the buffered mode. When the period is between 20 μs and 200 μs, the drive must be programmed to operate in the semi-buffered mode.

CHAPTER 3
THEORY OF OPERATION

3.1 General Description

This chapter consists of the following sections:

(1) Mechanical parts

(2) Servo surface information and data surface track format

(3) Interface and electrical control section

3.2 Unit Structure

The M224XAS consists of disks, heads, spindle motor, actuator, cover, recirculation filter, base, Read/Write pre-amplifier (PCB), power amplifier (PCB), and control (PCB). Refer to Figure 1.2.

(1) Disks
Disks are 130 mm in outer diameter and 40 mm in inner diameter and are coated with a special lubricating material (Winchester-type). M2241AS, M2242AS and M2243AS have 3, 4 and 6 disks respectively. Durability is designed for over 10,000 contact starts and stops.

(2) Heads
The Whitney-type heads are in contact with the disks when the disks are not moving, but automatically float when the rotation reaches nominal speed.
The number of heads (R/W) is four in the M2241AS, seven in the M2242AS, and eleven in the M2243AS. Each model has a single servo head to read a servo pattern pre-written at the factory on the bottom disk's lower surface.

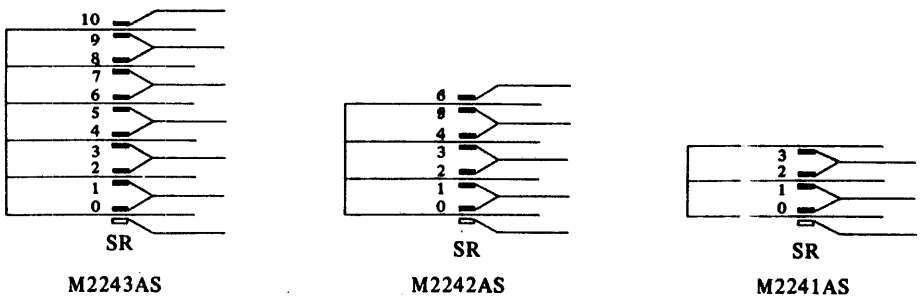


Figure 3.1 Disk/Head Configuration

(3) Spindle motor
The disks are turned by a direct-drive DC motor. The motor attains a very precise rotational speed of 3600 rpm, ±1%. This precision is achieved through a feedback circuit which includes Hall-effect elements mounted within the motor assembly.

(4) Actuator
This assembly consists of a rotary type actuator, moving coil, permanent magnet, and head arms with data heads and servo head.
The actuator which is controlled by a servo feed-back current, gives increased reliability and a very short average positioning time of 33 ms.

(5) **Air circulation**

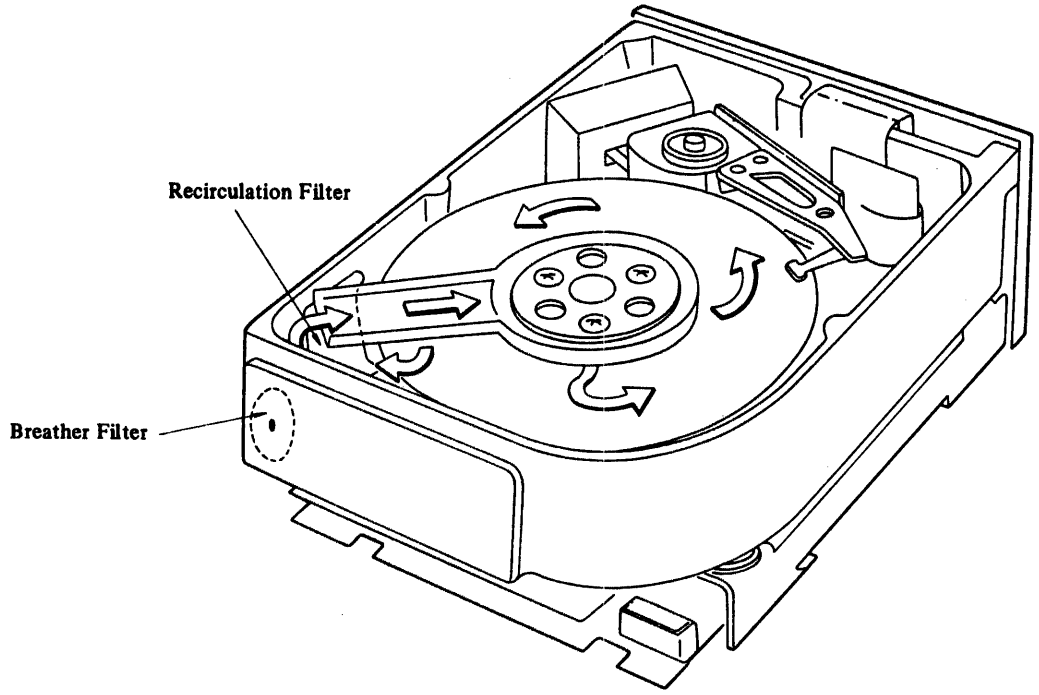


Figure 3.2 Air Circulation

As shown in Figure 3.2, the heads, disks and actuator are sealed inside a cover to shut out any contamination. This head disk assembly has a closed-loop air recirculation system using the blower effect of the rotating disks to continuously cycle air through the recirculation filter. This filter traps any dust generated inside the enclosure. To prevent negative pressure in the vicinity of the spindle when the disks begin rotating, a breather filter is attached. This breather filter also equalizes the internal air pressure with the atmospheric pressure due to surrounding temperature changes.

3.3 Recording Media

3.3.1 Servo track format

(1) Servo track configuration

The servo area is used to store the special data patterns which generate Track Positioning, Index, Guard Band, and Clock signals. This data is recorded on the disk before the unit is shipped from the factory.

The servo area consists of a combination of ODD1, ODD2, EVEN1 and EVEN2 tracks. The physical placement of servo tracks is shown in Figure 3.3. The servo tracks are divided into the following five parts:

a. Dead Space (DS)
DS consists of five DC-erased tracks and is recognized as Head Unloaded through the servo circuit.

b. Inner Guard Band 2 (IGB2)
Inner Guard Band 2 is used for speed control during Return To Zero (RTZ) or Initial seek sequence. IGB2 consists of six EVEN1-EVEN2 tracks, six ODD1-EVEN2 tracks, six ODD1-ODD2 tracks and five EVEN1-ODD2 tracks (23 tracks total).

c. Inner Guard Band 1 (IGB1)
Inner Guard Band 1 is located between IGB2 and Cylinder 0, and is used for speed control during RTZ or Initial Seek sequence. IGB1 consists of four EVEN1-EVEN2 tracks, four ODD1-EVEN2 tracks, four ODD1-ODD2 tracks and four EVEN1-ODD2 tracks (16 tracks total).

d. Servo Band
Servo Band is used for tracking to determine the center of each cylinder. The Servo Band consists of 189 EVEN1-EVEN2 tracks, 189 ODD1-EVEN2 tracks, 189 ODD1-ODD2 tracks, and 190 EVEN1-ODD2 tracks (757 track total). However, 1.5 inner tracks of Cylinder 0 and 1.5 outer tracks of Cylinder 753 are not utilized for corresponding data tracks.

e. Outer Guard Band (OGB)
The Outer guard Band is used to recognize that the head has passed through the servo zone in an outward direction. OGB consists of four EVEN1-EVEN2 tracks, four ODD1-EVEN2 tracks, three ODD1-ODD2 tracks and three EVEN1-ODD2 track minimum (14 tracks minimum total).

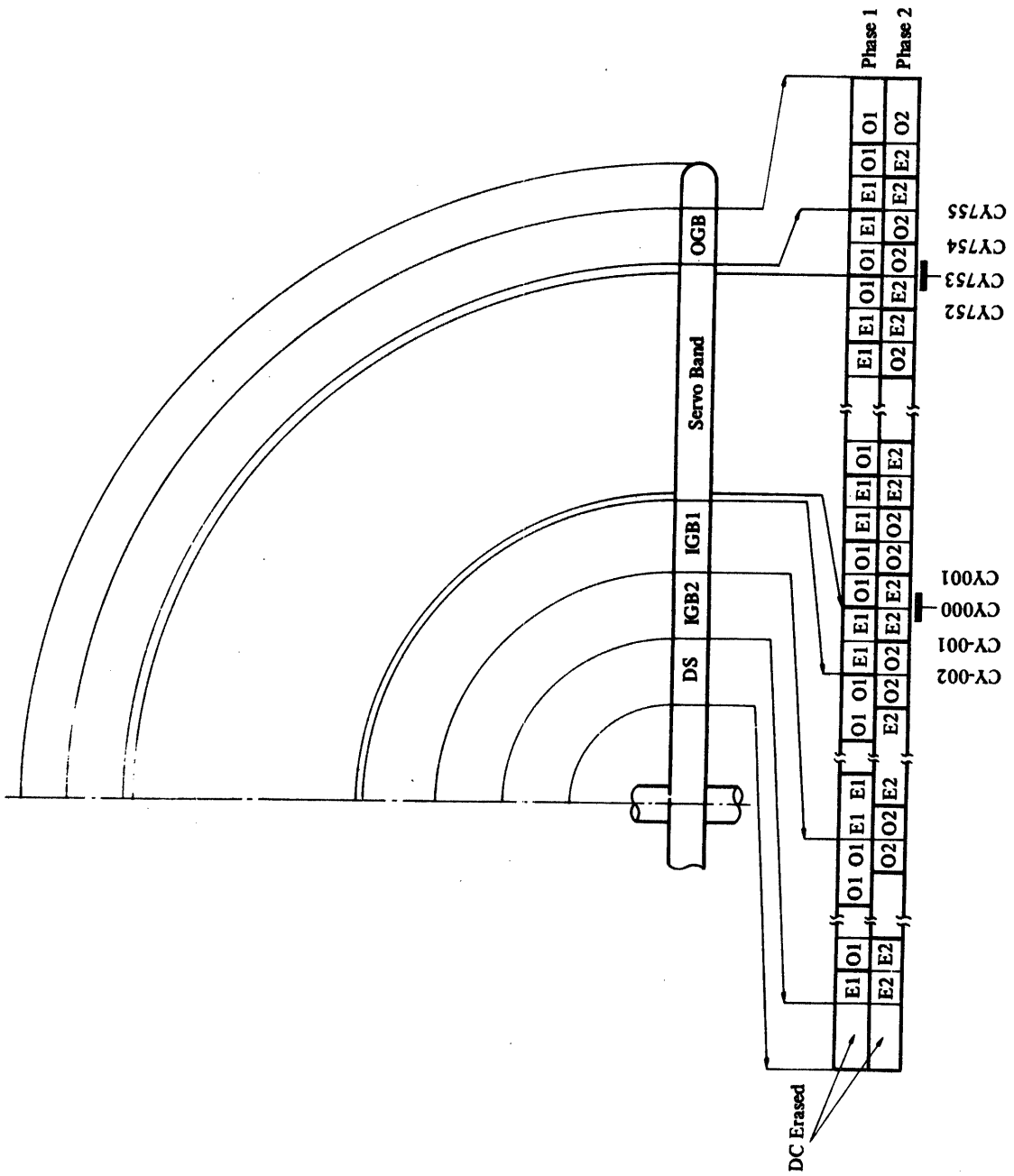


Figure 3.3 Servo Track Configuration

3.3.2 Servo pattern

The servo signal is a unique ''Dual-phase composite servo signal'' which creates a high-performance positioning system. It is used to achieve angular positioning (location with reference to the circumference of the disk) and radial positioning (location with reference to the radius of the disk).

Angular positioning is determined by a series of sync bits which are written on each track. Through a combination of Index Bit and Normal Bit, the ''sync pattern'' is developed. A series of unique sync patterns is written at the factory and used in the indentification of specific disk regions. Refer to Figure 3.4 and Figure 3.5

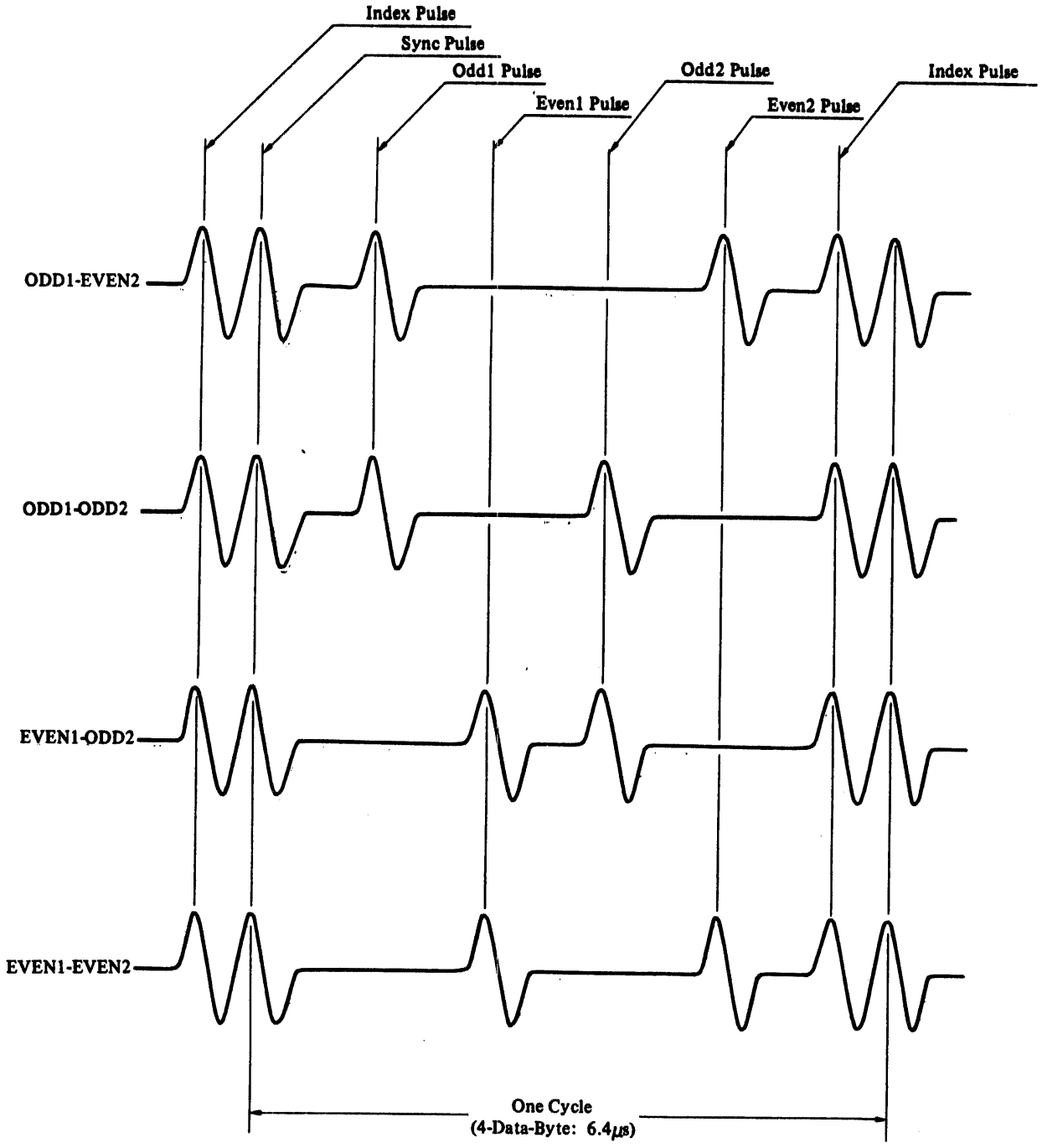


Figure 3.4 Normal Bit Pattern

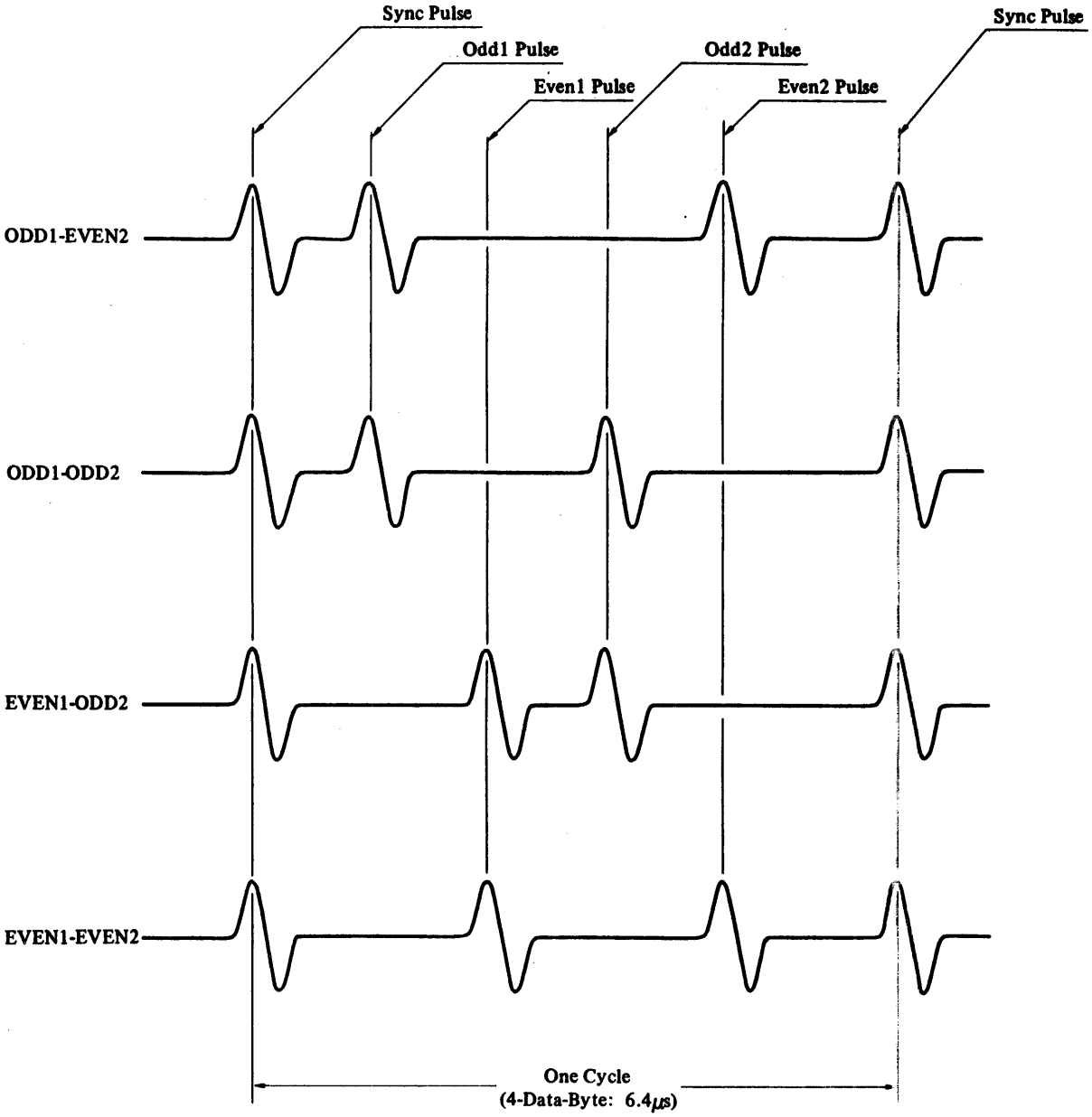


Figure 3.5 Index Bit Pattern

Radial positioning information is provided by writing ODD1–EVEN2, ODD1 –ODD2, EVEN1–ODD2, and EVEN1–EVEN2 patterns, in that order, on the servo surface.
During head movement, the servo circuit detects the amplitude changes between ODD1 and EVEN1 peaks (phase1), and between ODD2 and EVEN2 peaks (phase2), and then converts them into two position signals (phase 1: Normal, phase 2: Quadruture) through position sensing.
After head movement, the servo head, which has double the core width of the data head, settles on the border of two types of servo patterns controlled by the two least–significant bits of the target cylinder address. The servo circuit then makes the ODD1 (or ODD2) peak equal to the EVEN 1 (or EVEN2) peak by positioning the servo head on the center of the servo track. Refer to Figure 3.6.

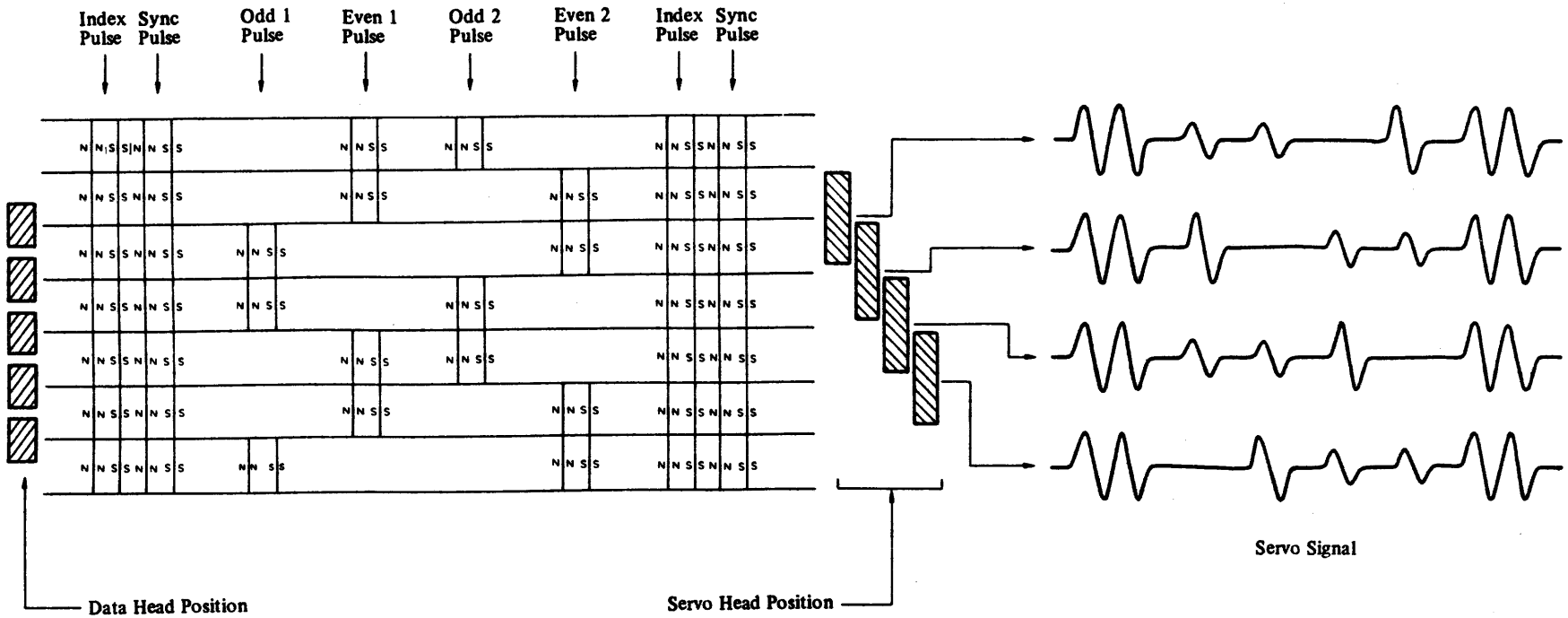


Figure 3.6 Dual-Phase Composite Servo Signal

3.3.3 Index guard band patterns

Index (INX), Sector (SCT), IGB2, IGB1, and OGB patterns are detected by decoding the combination of Index bits and Normal bits. Each of the patterns are shown in Table 3.1.

Table 3.1 Index, IGB2, IGB1, and OGB Patterns

Signal	Pattern	Pattern interval
Index	01011	10,416 B
SCT	01101	325 B
IGB2	01110	260 B
IGB1	01010	260 B
OGB	10011	260 B

Note: 0-Normal bit
1-Index bit

3.3.4 Data surface format

The data surface consists of 754 cylinders for data recording.
Cylinder 0 inner most and Cylinder 754 is the outer most data cylinder.

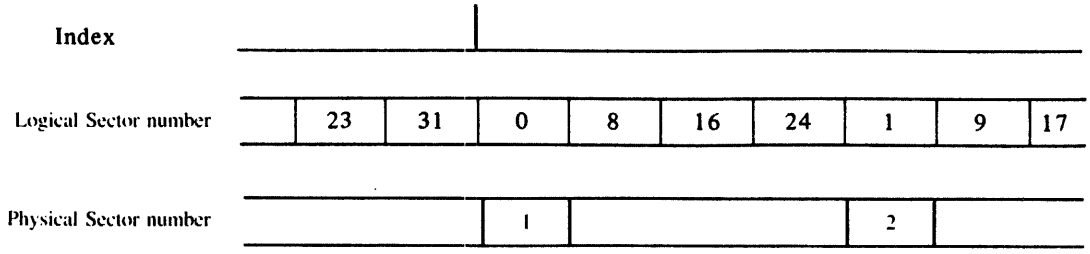
(1) Track format

a. General

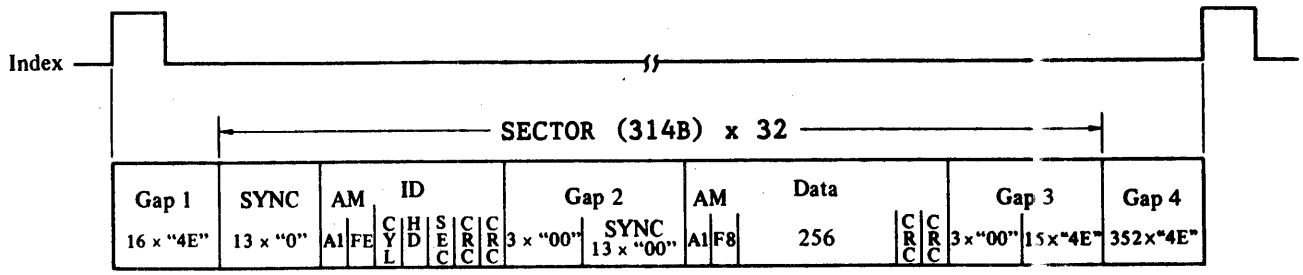
The soft sector format, which is the same as that for floppy disk drives, is used as the track format for these drives. Each sector consists of an identify (ID) field for checking that the correct sector is read and a data field for actually recording data.

The sector format is decided by the controller. This section explains the format written at the factory.

Sector interleave format (factor = 4) is set at the factory. A track has 32 sectors.



b. Track format written at the factory



Notes: 1. The track capacity varies according to the motor rotation fluctuation. The nominal track capacity is 10,416 bytes.
2. The nominal capacity of Gap 4 is 352 bytes.
3. 16 x ''4E''

Indicates the hexadecimal bit pattern.

Indicates the number of bytes.

(2) Format configuration

a. Gap 1

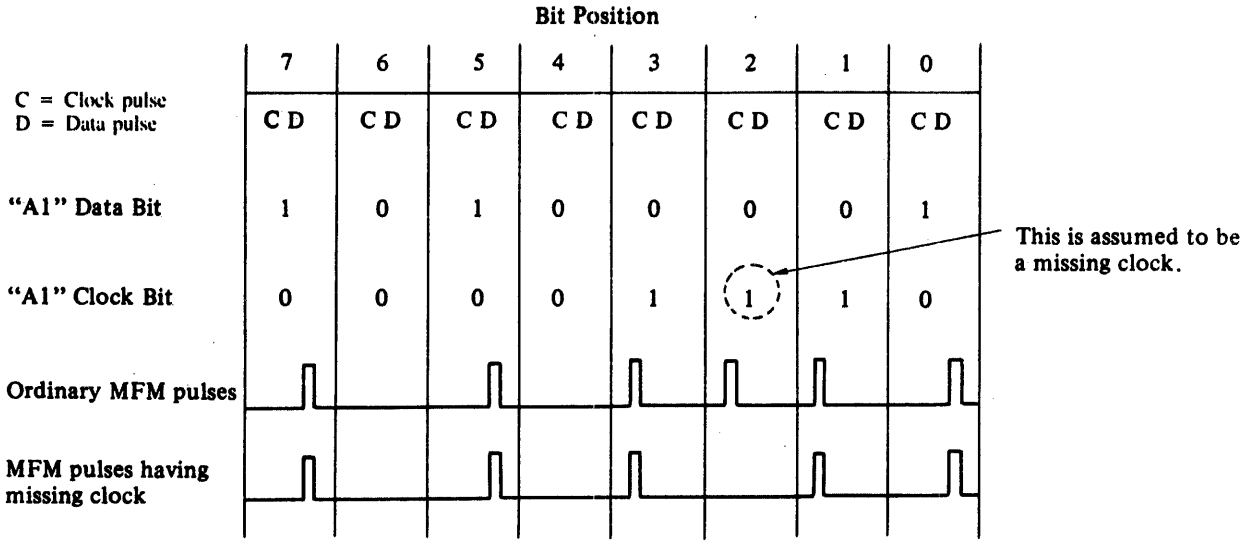
Absorbs the index burst fluctuation. Sixteen bytes of ''4E'' patterns are written in this gap.

b. SYNC

VFO synchronization area for reading the ID and data fields. Thirteen bytes of ''00'' patterns are written in this field.

c. Address mark (AM)

Identifies the heading part of the ID and data fields. ''A1'' patterns are written in the following missing clock format to detect the AM.

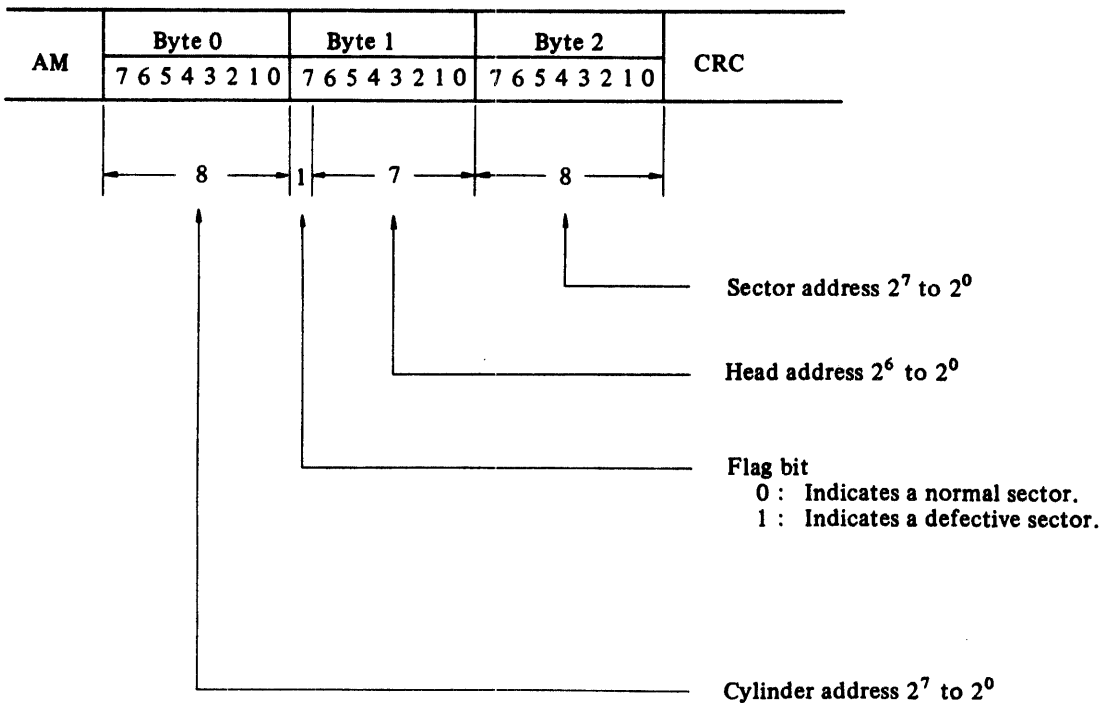


The data pattern of byte 2 succeeding the A1 pattern of AM as follows:

ID field:	FE at cylinders 0-255
	FF at cylinders 256-511
	FC at cylinders 512-753
Data field:	F8

d. Identify (ID) field

The ID field consists of seven bytes, including AM and CRC. The three bytes other than AM and CRC have the following bit configurations:



e. Cyclic Redundancy Check (CRC) field

Error detection code including AM (A1 pattern). The polynomial is as follows:

$$X^{16} + X^{12} + X^5 + 1$$

Note: The CRC initial value is FFFF.

f. Gap 2

Area for reading/writing the data field. The data pattern for synchronizing the variable frequency oscillator (VFO) is "00".

g. Data field

This is the user area.

h. Gap 3

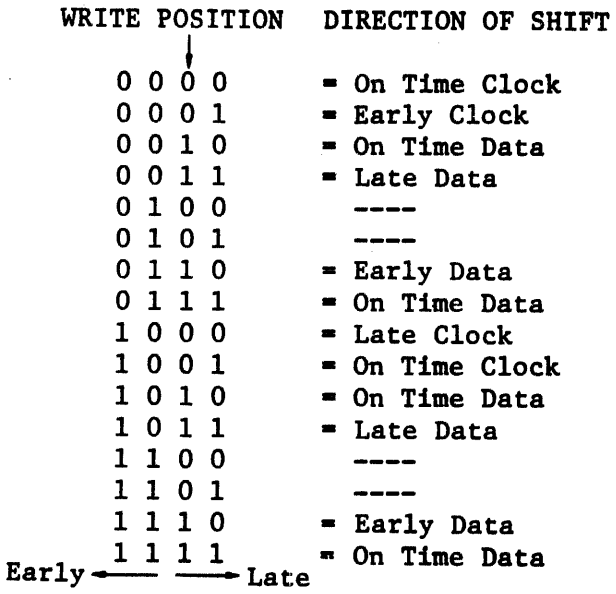
Consists of 3-byte "00" patterns for writing the data field and 15-byte "4E" patterns for absorbing motor rotation fluctuation.

i. Gap 4

Area for absorbing motor rotation fluctuation used when formatting all sectors in a track at the same time. This area consists of 352-bytes of ''4E'' patterns (nominal rotation number).

(3) Write precompensation

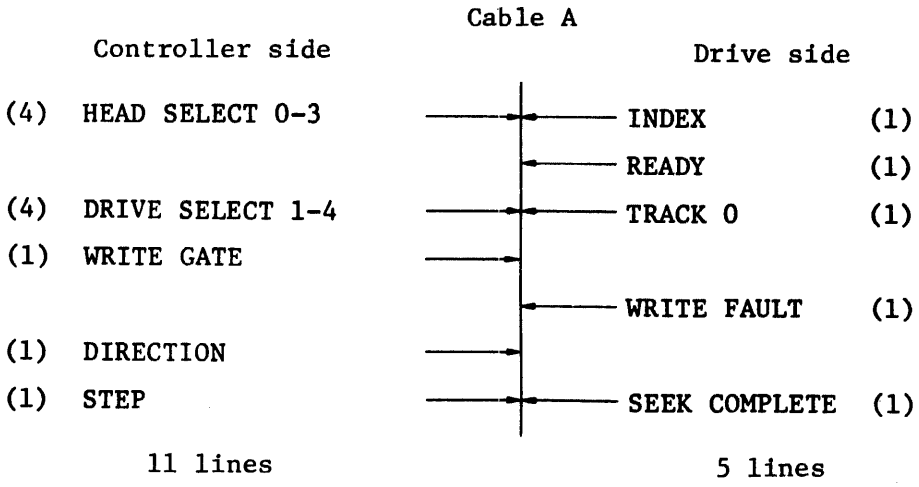
Whenever two bits are written in close proximity to each other, a phenomenon called pulse superposition occurs, which tends to cause the two bits to move away from each other. This factor contributes to bit shift. The effect of bit shift can be reduced by a technique called precompensation, which, by detecting which bits will occur early and which bits will occur late, can effectively minimize the shift by writing these bits in the opposite direction of the expected shift.
The optimum amount of pre-compensation is 12 nanoseconds for both early and late written bits. No precompensation is, however, required. The following table shows various bit patterns for precompensation.

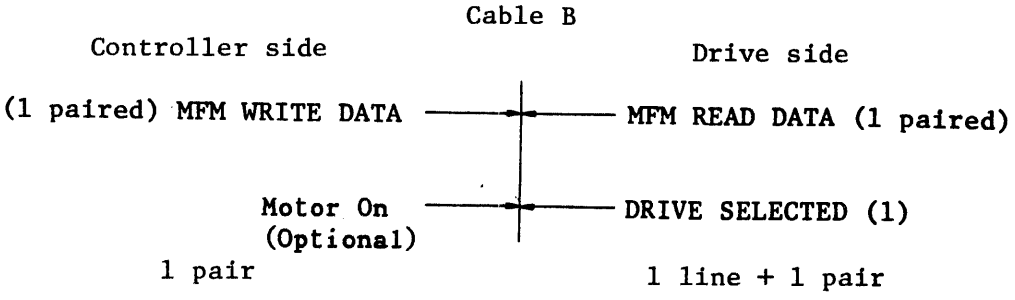


3.4 Interface

This section describes the physical and logical conditions of the signals transferred through the interface between the disk drive and the disk control unit. The timing is specified at the driver/receivers of the drive.

3.4.1 Signal Lines





3.4.2 Input signals

(1) Head Select 0 to 3
These signal lines are used to select one of up to eleven data heads in the disk drive.

(2) Drive Select 1 to 4
These signal lines are used to select from one of up to four drive units in a multi-drive configuration and validate the input/output signals of the selected disk drive.

(3) **Direction**
This signal line is used to determine the seek direction of the data heads when the step pulses are sent to the disk drive. When this signal is true, seek is performed away from Track 0; when false, seek is performed toward Track 0.

(4) Step
This signal moves the data heads one track per pulse in the direction indicated by the Direction signal. There are two stepping modes as follows:

(i) Slave step mode
When the step pulse rate is between 5 kHz and 3 MHz, the seek operation does not commence until all the step pulses have arrived and responds with the Seek Complete signal after completing all seeks.

Note) Step rates 5 kHz or less are prohibited.

(ii) Return to zero mode
When 754 or more step pulses are issued in slave step mode, the data heads will move to Cylinder 0.
If the controller does not use this Mode, the recalibrate function should be performed using the following procedure.

① Set the Direction to false.

② Send one step pulse.

③ Wait until the Seek Complete signal is TRUE.

④ Continue the procedure until the Track 0 signal is TRUE.

Note: An illegal step pulse which would position the heads outside of the recording zone or an internal seek fault will cause the drive to position the heads at Cylinder 0 automatically, using its internal recalibration procedure. The drive will then activate Track 0 and Seek Complete signals.

(5) Write Gate
This signal line enables the write current to the selected data head in the drive. When this signal is false (logical "1"), the Read Data from the disk is transmitted to the interface.

(6) MFM Write Data (balanced transmission)
This signal is a differential signal used to determine the flux change point of the data bit written on the disk.
When +MFM Write Data goes more positive than –MFM Write Data while Write Gate is active, a flux change occurs.
During a Read, this signal should remain inactive (+MFM Write Data should be more negative than –MFM Write Data).

(7) **Open Cable Detect**
A disconnected cable can be detected by sensing continuity between connector J1, Pin 16 and J2, Pin 7 which are shorted on the drive.

(8) **Motor-On Function**
When multiple drives are connected to a system, the +12V power supply may be overloaded. To prevent such a situation, a circuit was added which allows for power-up sequencing by the system.
The controller may send an enabling signal, Motor-On, over the 'B' cable (Pin 5).

3.4.3 Output signals

(1) Index
This is a pulse signal generated once per revolution of the disk in the selected drive.

(2) Ready
This signal is true or zero when the voltages are within specification and the spindle motor has reached nominal speed. This signal is true approximately 20 seconds after power on.

(3) Track 0
This signal indicates that the data heads are positioned at Cylinder 0.

(4) Write Fault
This signal is true when one of the following abnormal states occur during writing.
(i) Either +5 V or 12 V drop below specification.
(ii) Write current is not applied to the head while Write Gate is enabled.
(iii) Write Gate is enabled during a multihead select condition or while no head is selected.
(iv) Write current flowed but Write Gate is not applied.
(v) Off track condition occurs.

(5) MFM Read Data (balanced transmission)
This signal is a differential signal used to send the Read Data bit from the disk to the host side. When the Write Gate is inactive, the point at which +MFM Read Data goes more positive than –MFM Read Data represents a flux reversal on the track of the selected head.

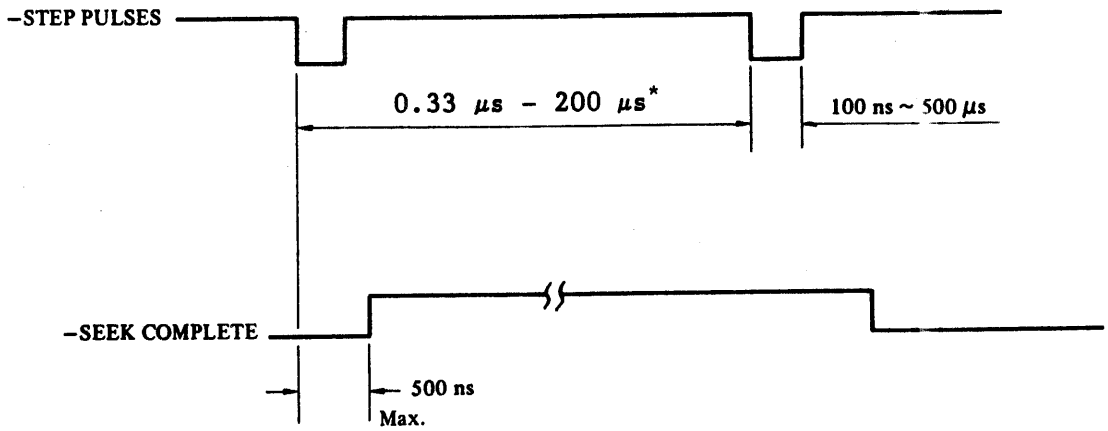
(6) Seek Complete
This signal indicates that the selected data head is positioned at the requested track. This signal includes the settling time of the head, and when it is true, read/write operations are enabled.

(7) Drive Selected
When the Drive Select 1 - 4 matches the Drive Select keys (DRSL 1 - 4) on the drive side, the drive is selected.

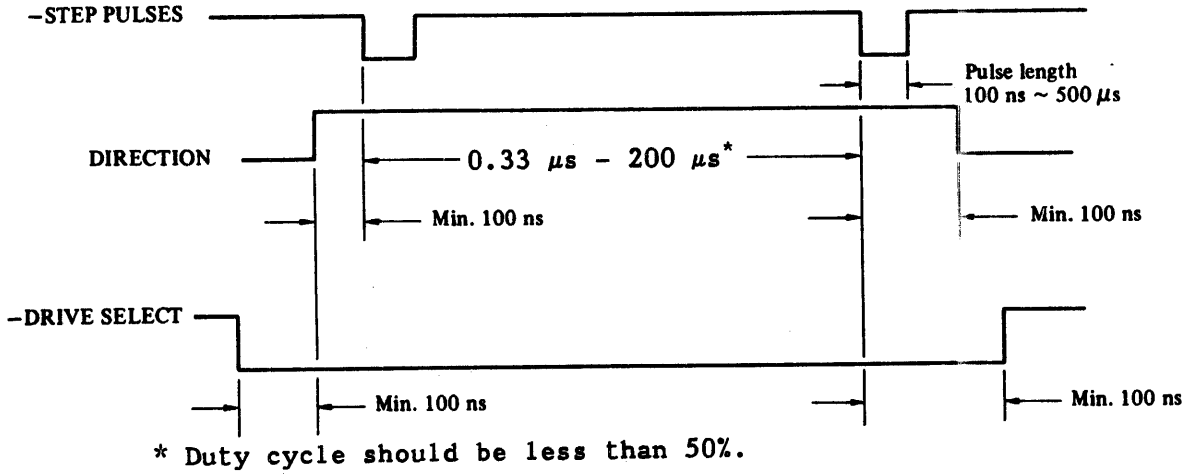
3.4.4 Timing specifications

(1) Seek timing

a. STEP/SEEK COMPLETE RELATIONSHIP



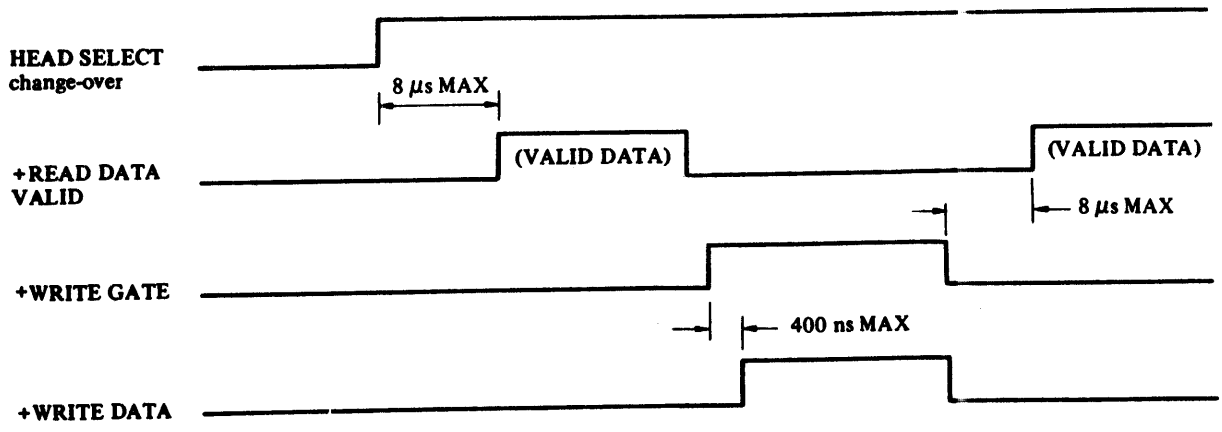
b. SLAVE STEP MODE



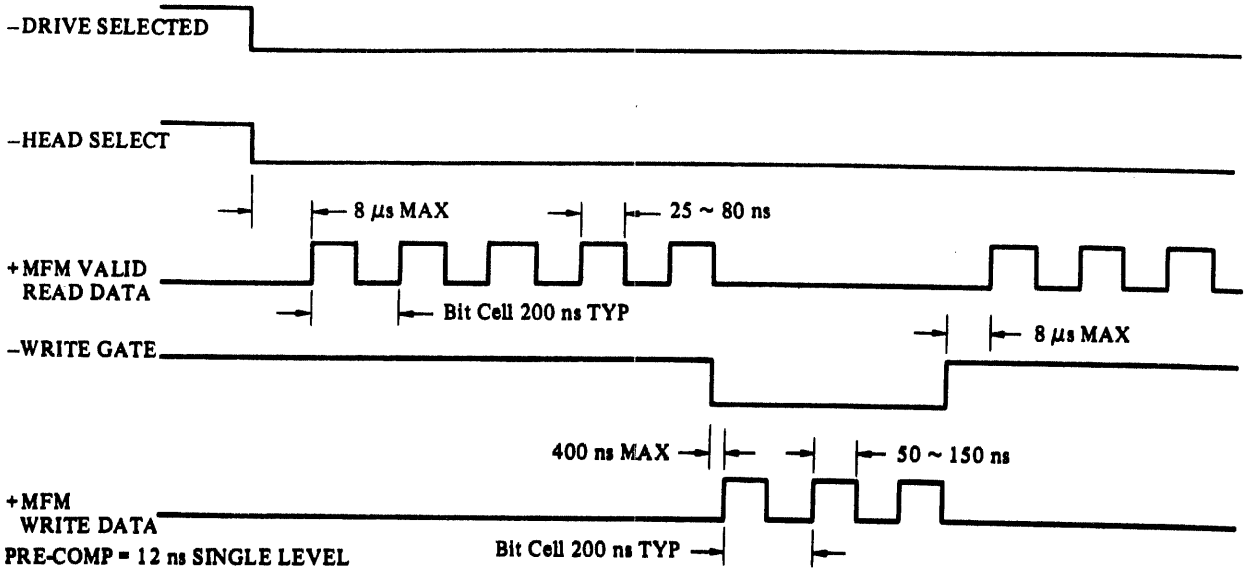
* Duty cycle should be less than 50%.

(2) Write/Read Data Timing

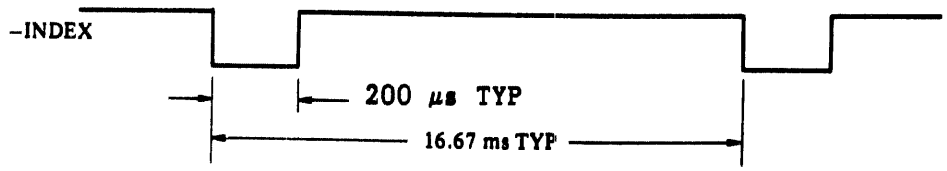
a. Head Change-over Timing



b. Read/Write Data Timing



(3) Index Signal Timing



3.4.5 Driver/Receiver

The interface signals are terminated as in Figure 3.7. The total control cable length in a multi-drive configuration should not exceed the specification.

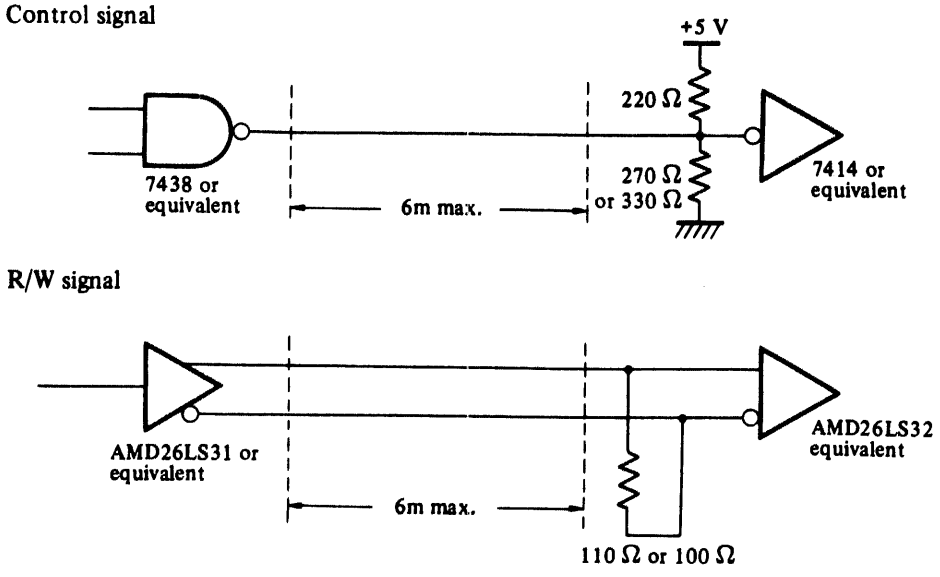


Figure 3.7 Driver/Receivers

3.4.6 Connector positions

a. ''A'' Connector (CNA)

1	GND	*2	-HEAD SELECT 3
3	GND	4	-HEAD SELECT 2
5	GND	6	-WRITE GATE
7	GND	8	-SEEK COMPLETE
9	GND	10	-TRACK 0
11	GND	12	-WRITE FAULT
13	GND	14	-HEAD SELECT 0
15	GND	16	(To 'B' - P-7)
17	GND	18	-HEAD SELECT 1
19	GND	20	-INDEX
21	GND	22	-READY
23	GND	24	-STEP
25	GND	26	-DRIVE SELECT 1
27	GND	28	-DRIVE SELECT 2
29	GND	30	-DRIVE SELECT 3
31	GND	32	-DRIVE SELECT 4
33	GND	34	-DIRECTION

Key slot: Between 4P and 6P

b. ''B'' Connector (CNB)

1	- DRIVE SELECTED	2	GND
3	RESERVED	4	GND
5	Motor-On (Optional)	6	GND
7	(To 'A' - P-16)	8	GND
9	SPARE	10	SPARE
11	GND	12	GND
13	+ WRITE DATA	14	- WRITE DATA
15	GND	16	GND
17	+ READ DATA	18	- READ DATA
19	GND	20	GND

Key slot: Between 4P and 6P

*In the M224XAS drives, pin 02 of cable A is used as -HEAD SELECT 3. However, this signal line is used as -REDUCED WRITE CURRENT in some disk controllers. Therefore, if such a controller controls M2241/2AS (number of HEADs 4/7), a

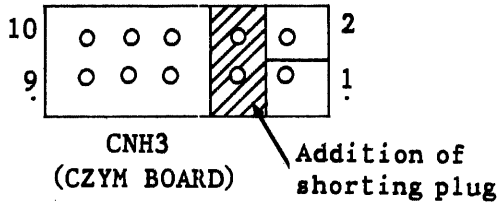
head selected for a cylinder number more than a certain value causes REDUCED WRITE CURRENT to be sent which then interferes with normal read/write functions.

For this reason, the -HEAD SELECT 3 signal was changed to be plug selectable. The drive can now be controlled by the above-mentioned controllers.

Plug setting method

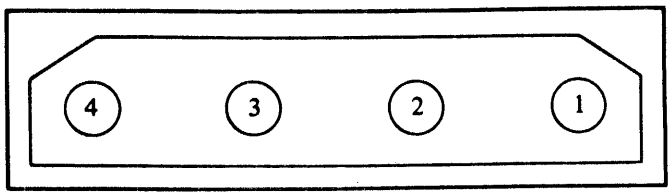
(1) Shorting plug is inserted between CNH3-3 and CNH3-4.
(Set when shipping from factory)
"Interface cable A is used as -HEAD SELECT 3."
(For M2243AS, the setting must be as above.)

(2) Shorting plug is inserted between CNH3-1 and CNH3-2.
"Interface cable A is used as -REDUCED WRITE CURRENT."
(-REDUCED WRITE CURRENT function is automatically performed in the device.)



c. Power Connector

CNC



From cable side

1	+12 V
2	+12 V RTN
3	+5 V RTN
4	+5 V

3.5 Theory of Operation

3.5.1 General description

The M224XAS is controlled by the microprocessor (MPU) (Intel 8031) and the sequence program stored in the EPROM (4K bytes). This section explains the operation of the M224XAS using block diagrams and the flowchart of the MPU sequence. Figure 3.8 shows the block diagram of the MPU control system.

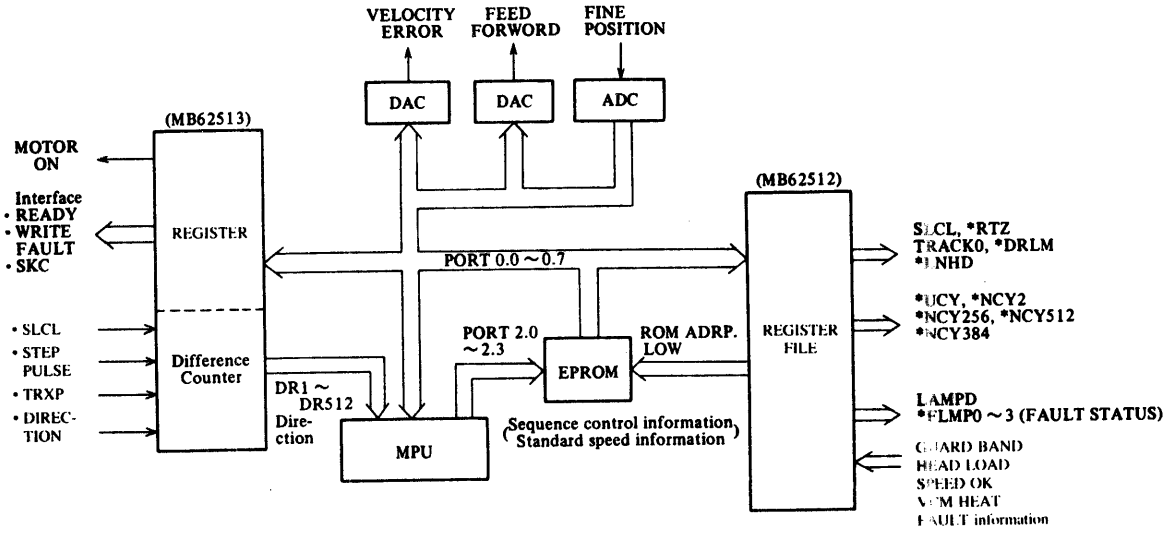


Figure 3.8 MPU Control System Block Diagram

3.5.2 Sequence

Figure 3.9 shows the flowchart from power-on, via drive ready, to the instruction executing sequence.

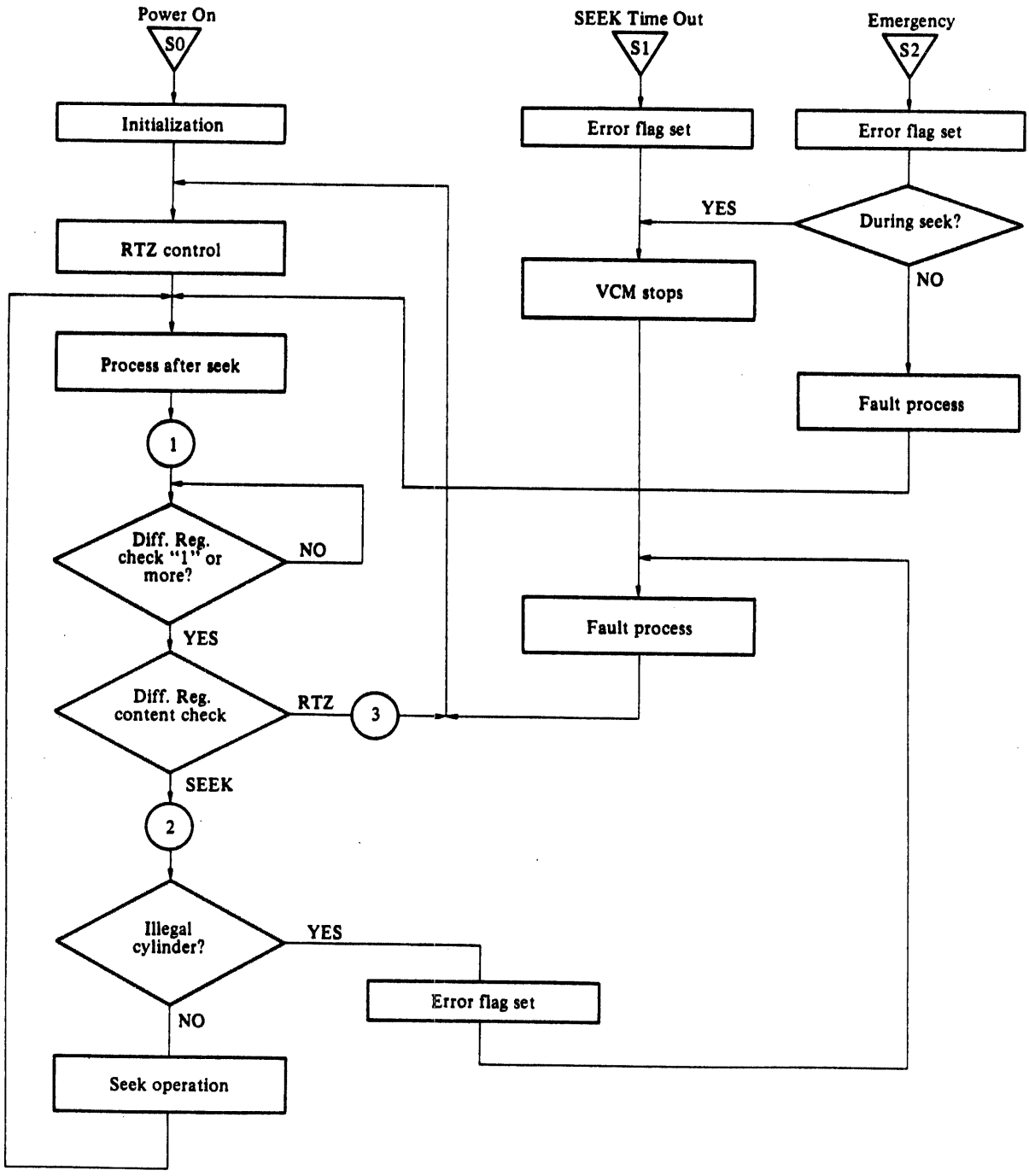


Figure 3.9 Control Flowchart

As shown in Figure 3.9, at power on, initialization (zero-clearing each memory and register) and RTZ operation of the initial seek sequence are performed. After RTZ operation, several processes (Ready, SKC and TRACK 0 process) are performed and the flow indicated by ① is entered. Difference register check is idling and awaits a seek instruction from the controller. As mentioned in the interface section, this register stores the number of the step pulses (actually difference value) under the slave mode, and sends it to the MPU. If that number is equal to or more than 754, the seek instruction is converted into an RTZ instruction. If less than 754, it is processed as a seek instruction.
Routines ② and ③ are determined by the content of the difference register.

Difference < 754 . . . . . enter into ② seek operation routine
Difference > 754 . . . . . enter into ③ RTZ operation routine

This flowchart is a basic operation. Therefore, when a time out or emergency condition occurs in this sequence, the normal sequence is stopped by interruption and the abnormal process routine is entered. As a result, the fault status is indicated by the status LED's. The MPU does not intervene directly with read/write operation.

3.5.3 Power-on sequence (initialization)

When +5V power is turned on, the MPU begins to operate and the following is performed:

- Reset each register in MPU
- Reset servo control register
- Reset each register of each sequence
- Reset each status register

Also, Motor On signal in the register in MB62513 is set, and the spindle motor control circuit begins to operate. Start up time is monitored by the 30 second counter in the MPU. Speed OK signal via MB62512 will be available if motor is up to speed within 30 seconds.

When Speed OK signal goes to ''1'', RTZ operation of the initial seek sequence is performed after 5 seconds. If the initial seek is not terminated within 30 seconds after powering-on, the spindle motor stops (Motor On signal is reset) and Fault code 03 is indicated by the fault lamp. This status is reset only by turning off and re-turning on the +5V power. Figure 3.10 shows the flowchart from power-on process to RTZ sequence.

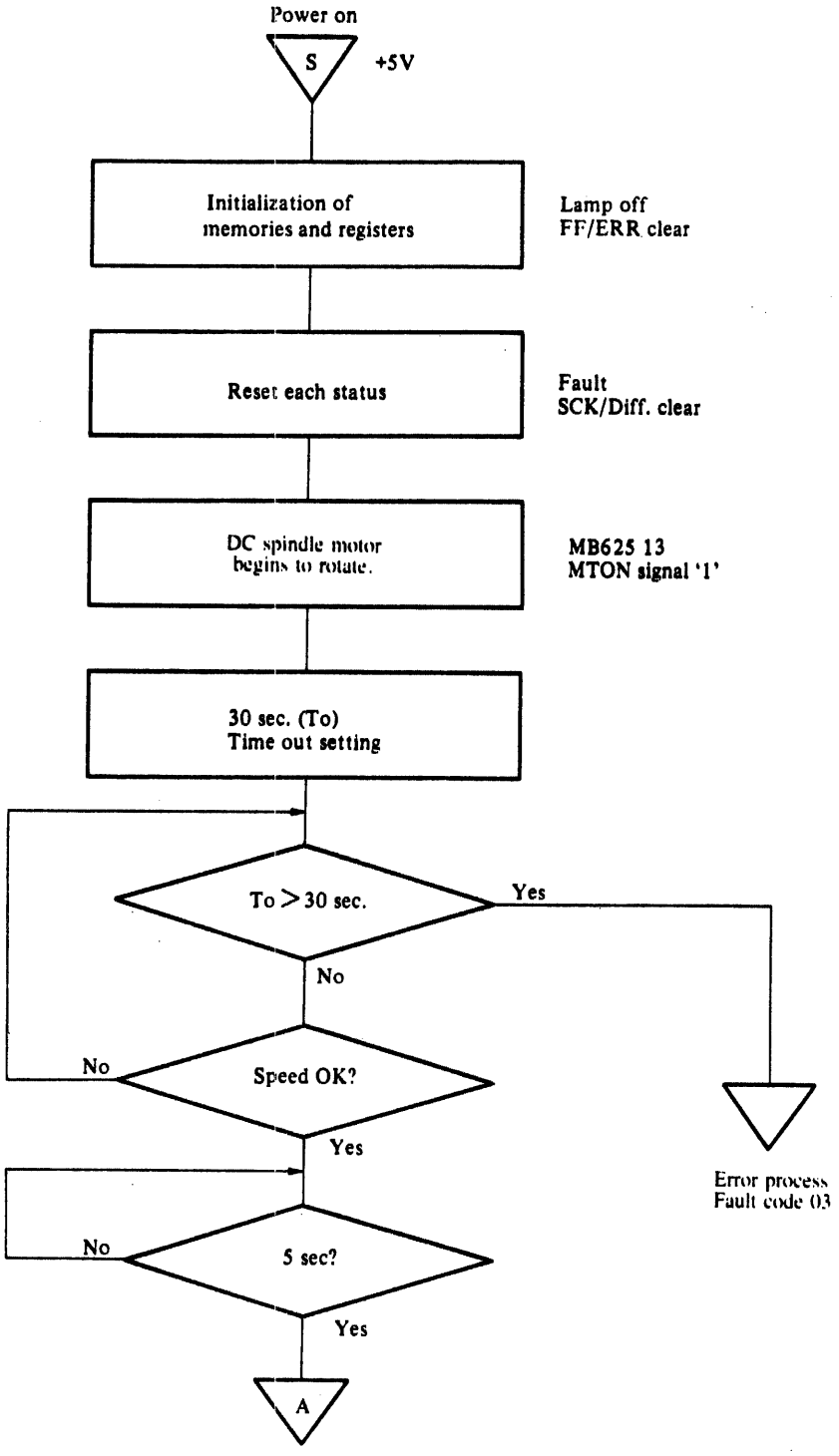


Figure 3.10 Power-On Sequence (Initialization)

(1) DC spindle motor control

Figure 3.11 shows the block diagram of the spindle motor control.

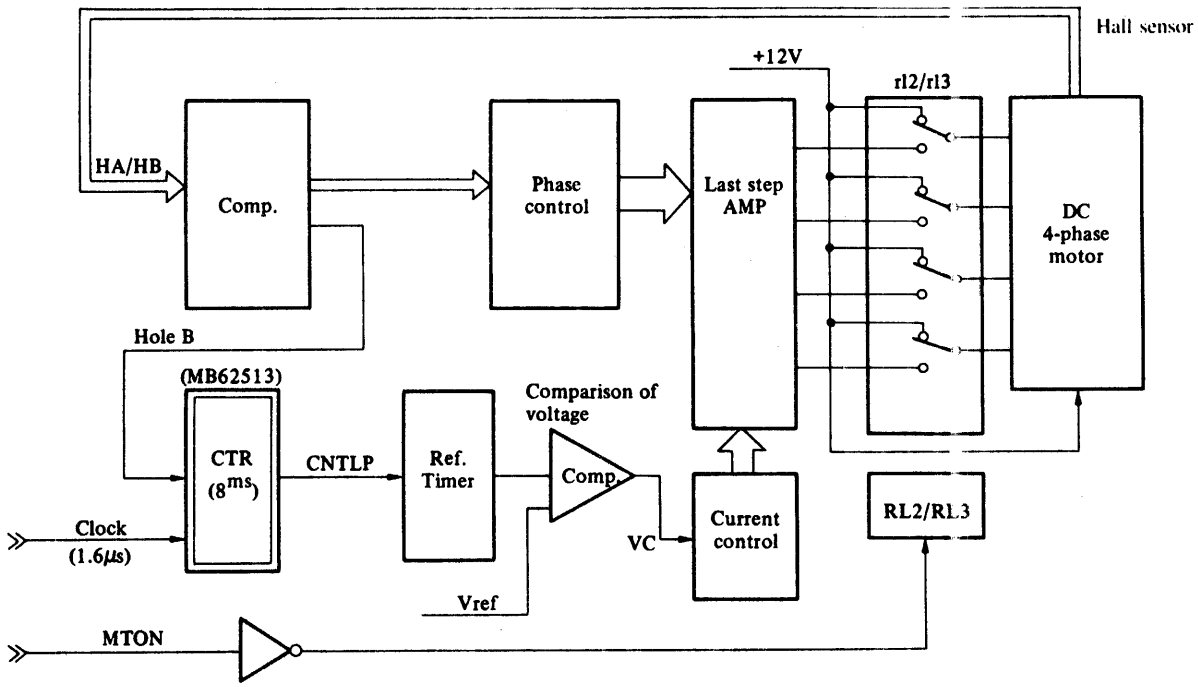


Figure 3.11 DC Motor Control Block Diagram

When powering off, the coil of the DC motor is shorted by the relay contact of the rl2/rl3 and the DC motor is in the dynamic brake status. Refer to Figure 3.12. Four lead wires of four coils and the common wire exit out of the DC motor and the common wire is connected to the +12V power. Two Hall sensors (HA, HB) are mounted in the DC motor to detect motor rotation.

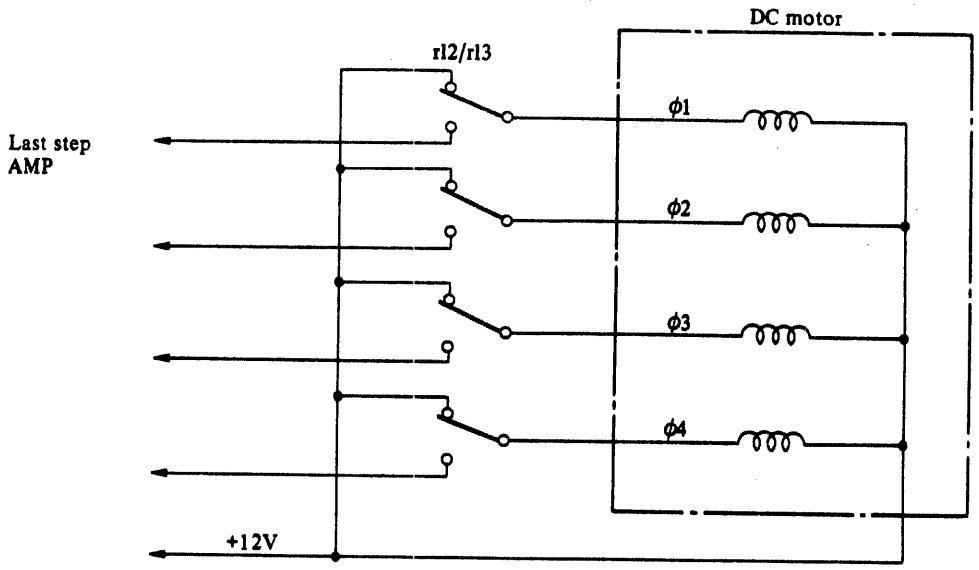


Figure 3.12 DC Motor Dynamic Brake

When the power is turned on and the MPU issues the motor start instruction (MTON), the contact of the relay (rl2/rl3) is switched to the last step AMP of the motor control circuit. The current control circuit flows the maximum current to one of four phases (ϕ1 to ϕ4) selected by the phase control circuit. The phase control is performed by the output signals (HA/HB) from the hall sensors. Output signal (HOLB) from the hall sensor operates the counter for controlling the DC motor rotation, and generates the signal (CNTCP) to the basic time (8 ms). This signal is used as the input signal of the basic timer circuit, and the voltage corresponding to the rotational time is the output of this circuit.
This output voltage is compared with the basic voltage (Vref) and is used as the input signal to the current control circuit. The output voltage of the counter is controlled to produce the same level as the basic voltage in case of the steady-state rotation. That means, when the output of the voltage comparison circuit is near 0V (steady-state rotation), the DC motor current control circuit stops the flow of current to the DC motor at the last step AMP. Figure 3.13 shows the timing chart.

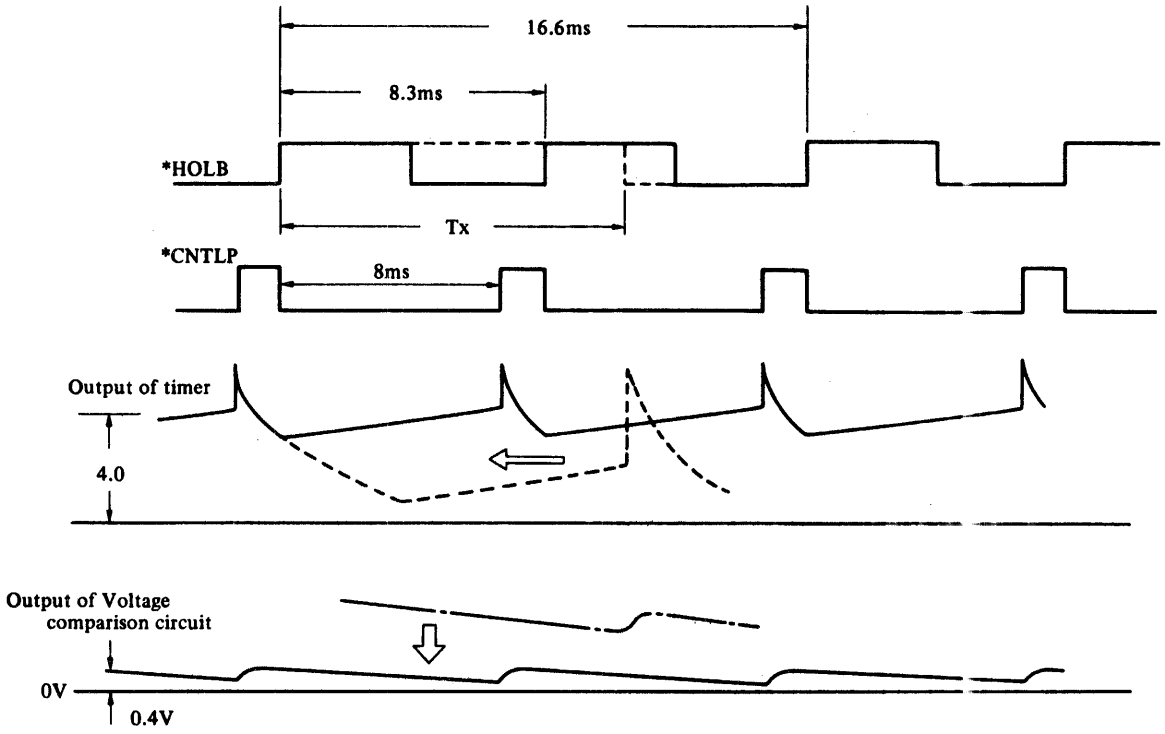


Figure 3.13 Steady-State Rotational Timing

When starting the DC motor, the waveform shown by the broken line in Figure 3.13 appears. This is the transition state. Figure 3.14 shows the waveform of the current control voltage Vc.

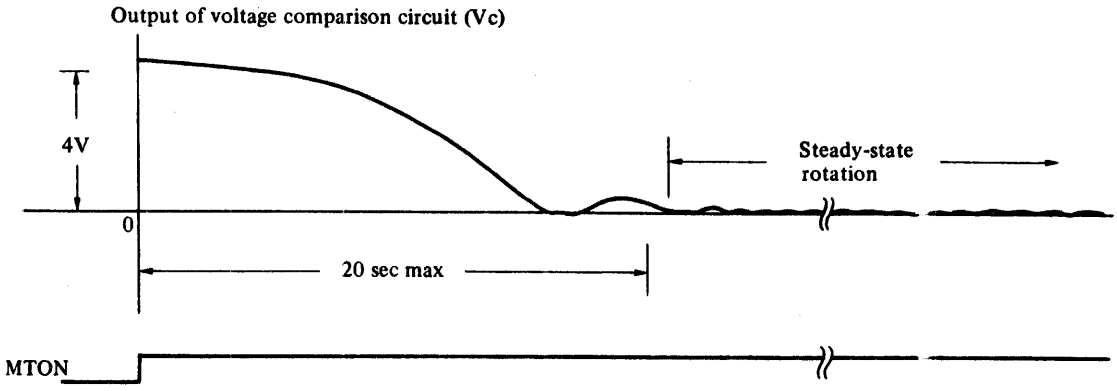


Figure 3.14 Current control voltage Vc

(2) Speed OK (SPDOK) signal sequence

HOLIN signal, given by differentially calculating the trailing edge of the output signal (HOLB) from the hall sensor, generates the CNTLP signal having the basic time (8 ms) in LSI MB62513. SPDOK signal is set when one-shot (approx. 1 ms) is triggered to the leading edge of CNTLP signal and the trailing edge of CNTLP signal that appears within this 1 ms. SPDOK signal is set at approximately 92% of the standard rotational speed, and after 5 sec, the initial seek (RTZ) is executed. Figure 3.15 shows the timing chart.

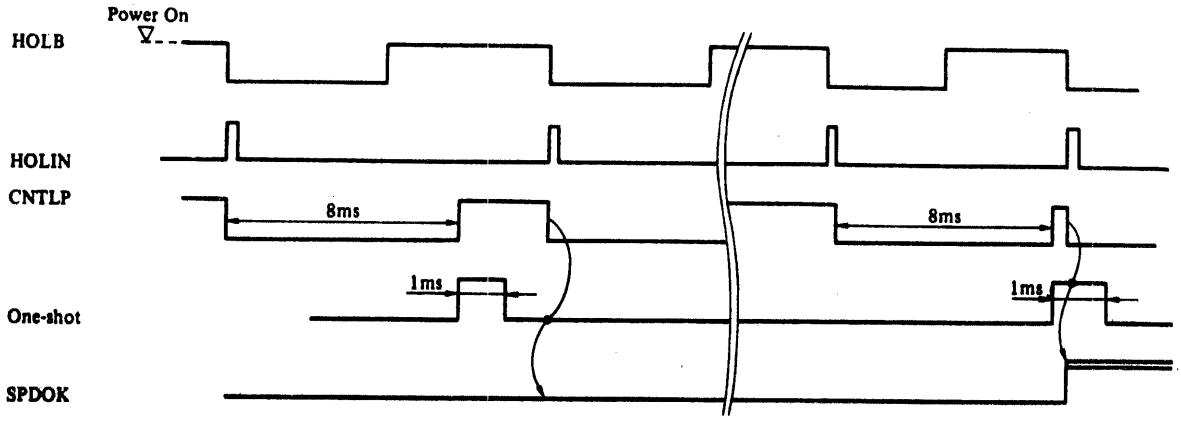


Figure 3.15 SPDOK signal timing chart

3.5.4 RTZ sequence

RTZ sequence makes the actuator move to Cylinder 0, and is executed in two cases: (A) Initial sequence after power on, (B) receiving an RTZ instruction.

In the RTZ sequence, the following process is executed.

(1) Time out setting (preparation of interruption)

(2) SKC resetting

(3) DRLM setting

Next, confirmation of HDLD, i.e. the head is already located in the servo area, is achieved. If HDLD is 0, moving direction becomes forward and the actuator is moved to outer direction at high speed until IGB2 is detected. After IGB2 is detected, the actuator is switched to low speed, and is controlled until IGB1 becomes false. When IGB1 becomes false, the two track seek routine begins, (IGB1 becomes false two tracks before Track 0.) When HDLD is 1, it means that the heads are in the servo area. In this case, if the heads are in IGB2 area, the flow enters the above routine. If in another area, it is moved in the reverse direction (inner) at high speed until IGB1 is detected. After IGB1 is detected, the actuator is switched to low speed, and is controlled until IGB2 is detected. After detecting IGB2, the flow enters the sequence already mentioned. If a fault occurred during this sequence it is indicated by the LEDs on the PCB.

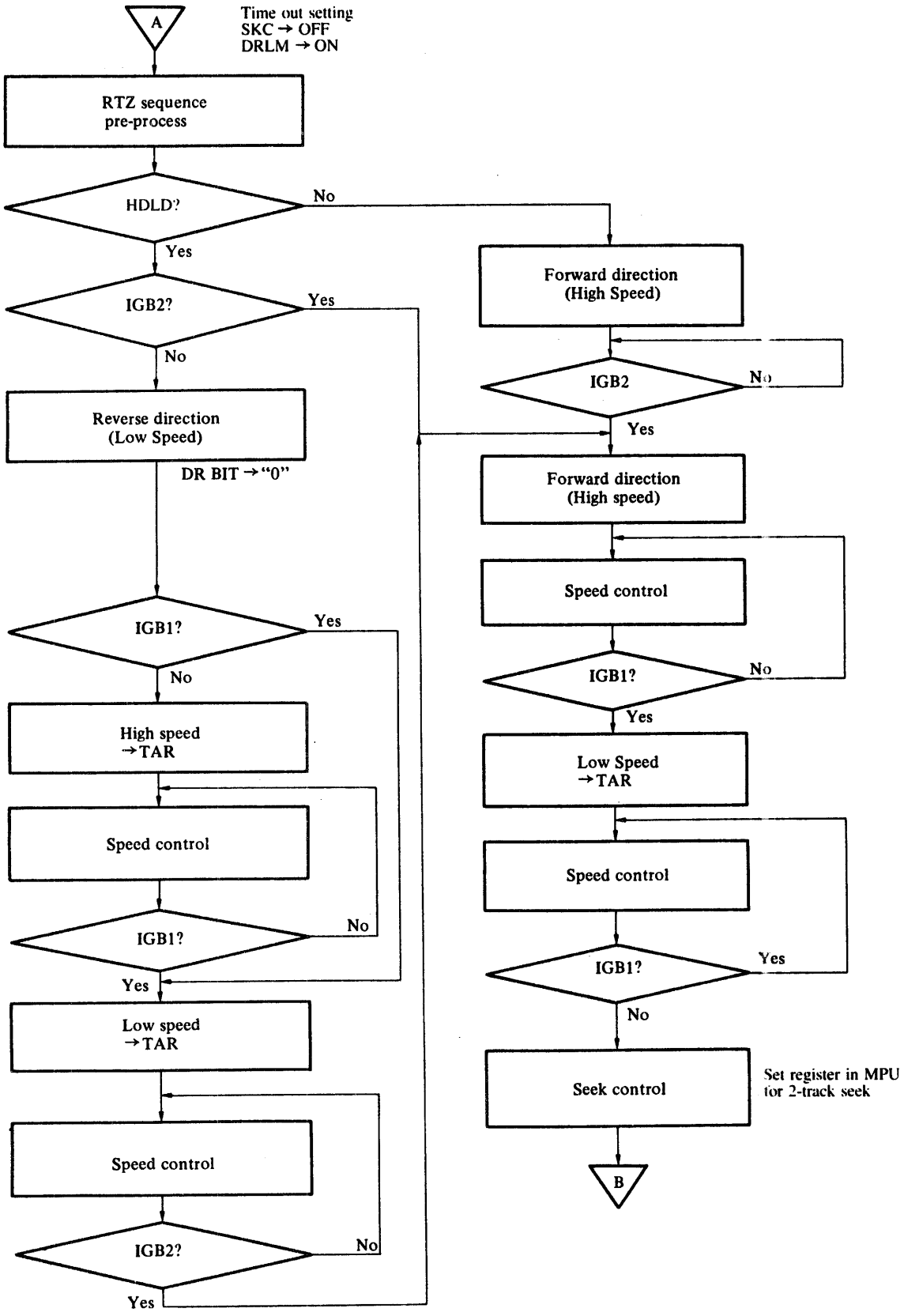
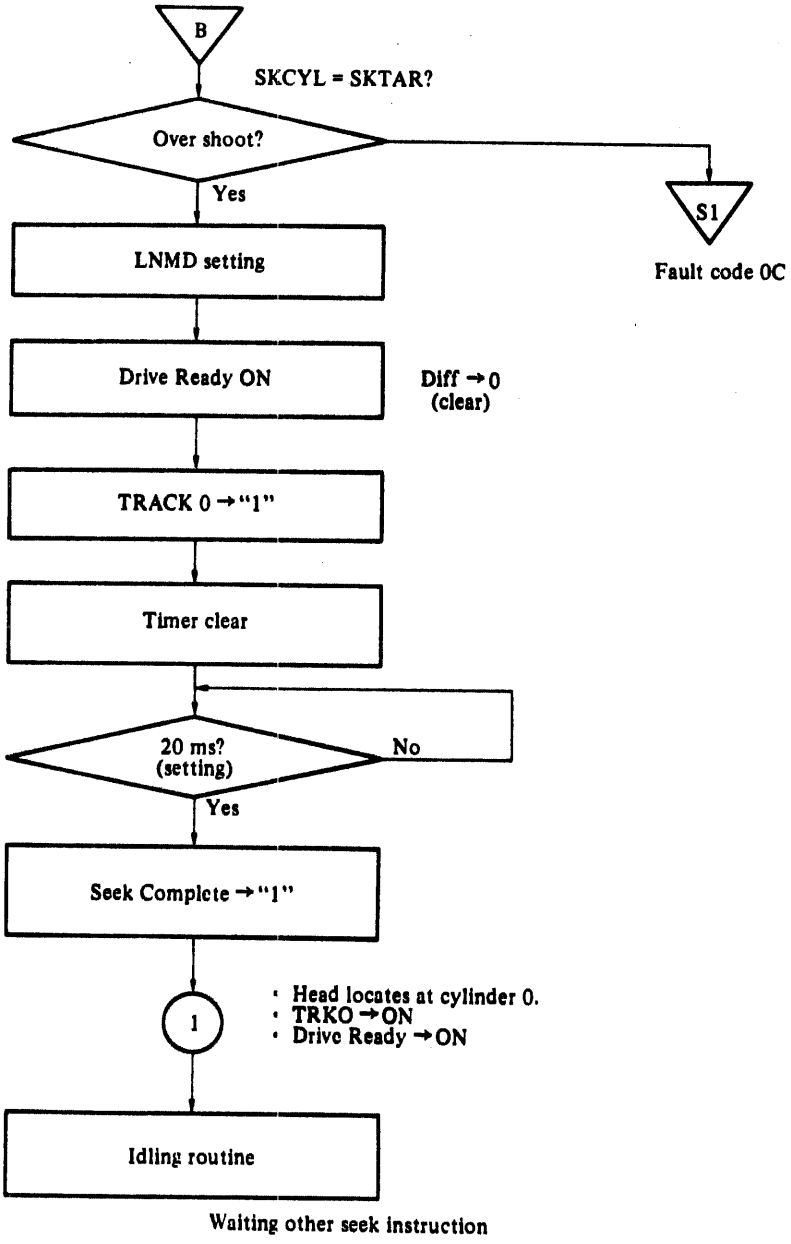


Figure 3.16 RTZ sequence



Note: SKCYL: Current address
SKTAR: Target address
TAR: Target speed

Figure 3.17 Post Seek Sequence

3.5.5 Seek sequence

The seek sequence consists of the seek pre-process, the seek speed control and the seek post-process.

In the seek pre-process, the following is executed and controlled by the direction and number of step pulses given by the interface.

- Illegal cylinder check
- DRLM, SKC, *NCY1, *NCY2 setting
- Seek-time-over timer starting
- Initial feed forward value setting

In the seek speed control, the current position is read and the difference value to the target cylinder is calculated. If the difference is 0, the flow enters into the seek post-process. If the difference is 1, the speed control is performed. The speed control is achieved by the following procedure:

① Calculate the difference between the current location and the last location ($\Delta v=\Delta x/\Delta t$, Δt: calculated cycle time).

② Read the target speed corresponding to the difference value from EPROM.

③ Set the speed difference between the current speed and the target speed.

The current location is determined by analog-to-digital convertion of the -Fine Position signal which indicates the detailed location between tracks. The difference counter stores the track crossing pulses (TRXP).

To stabilize decreasing speed control of seek, Feed Forward signal is active through the DA converter. This signal is not output when the difference value is more than 128, and is active from the point that the current speed exceeds the target speed until seek stops when the difference value is less than 128. When the difference value is less than 20, the feed forward value is decreased in each calculating cycle. Therefore, it is available to decrease the speed gradually.

The seek post-process is the same as RTZ. Figure 3.18 shows the seek sequence flowchart.

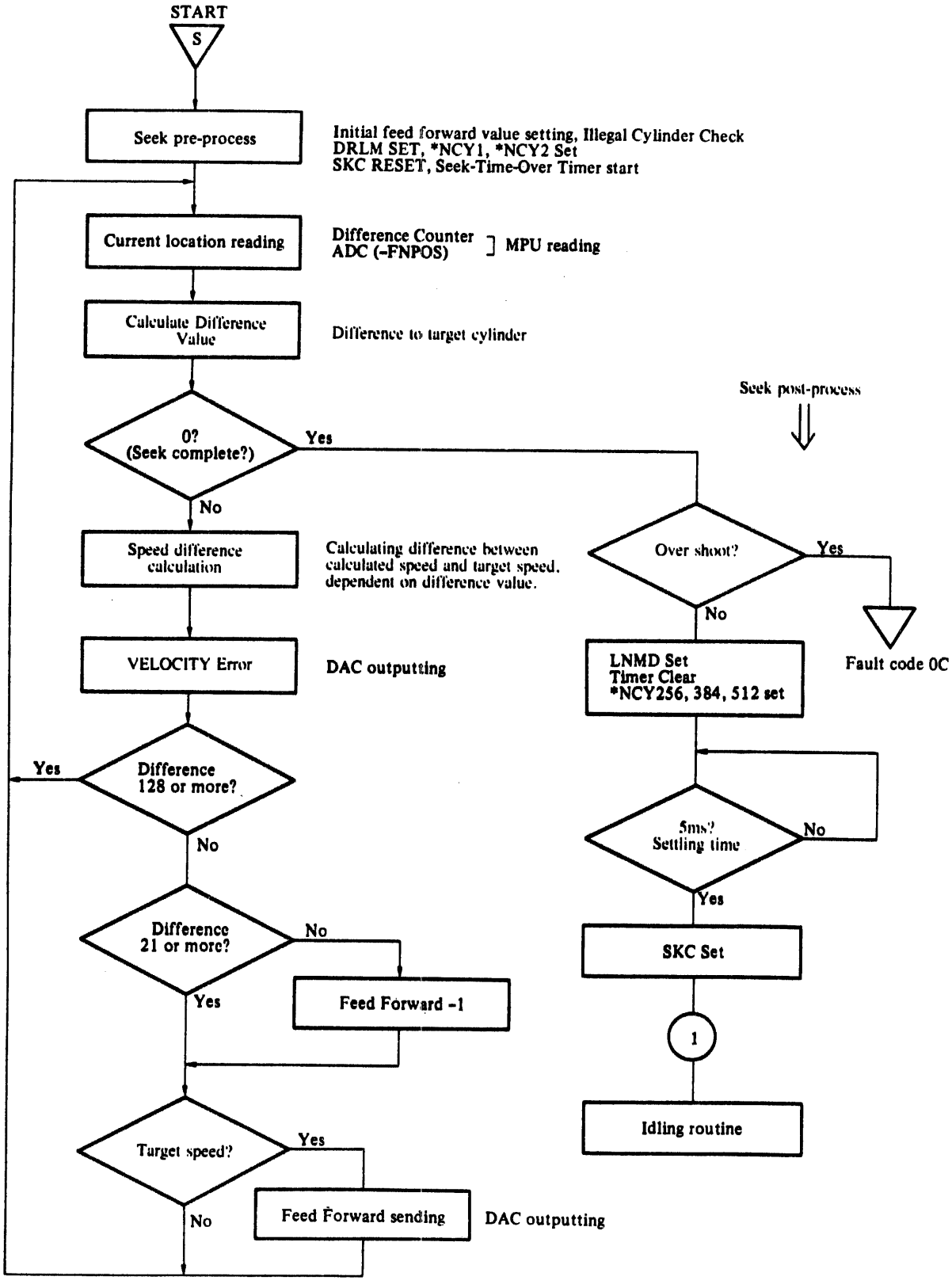


Figure 3.18 Seek Sequence

3.5.6 Seek control circuit

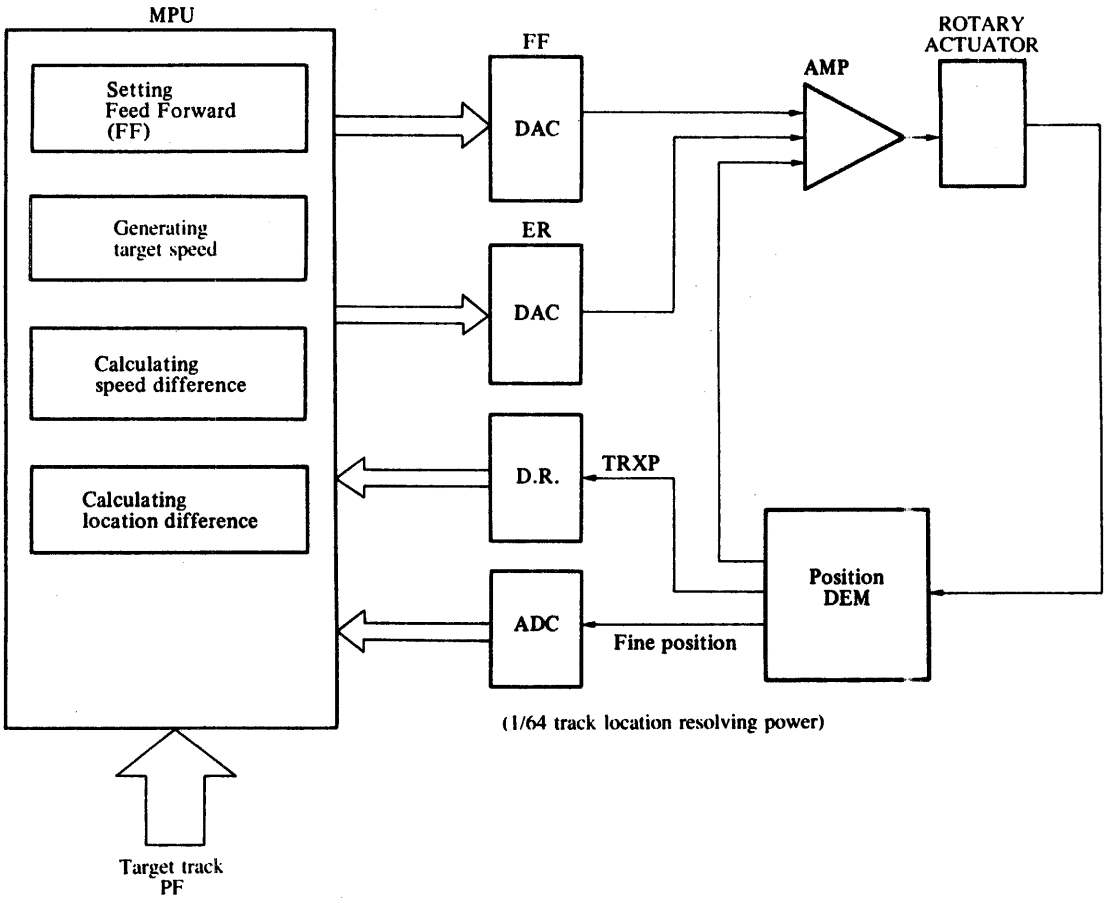


Figure 3.19 Seek Block Diagram

Figure 3.19 shows the block diagram of the seek circuit. The microprocessor (MPU) sets the feed forward value and enables current to the actuator with the ER signal. This feed forward value is an assumed value set with available information. The forecast value of the necessary current to move the head to the target track is given by the circuit different from the feed-back circuit, and the speed difference is set to 0 through the decreasing speed area, and the actual speed is made to coincide with the standard speed. Therefore, the difference between the actual speed and the target speed occurs. If it is necessary to correct the actual speed, that information will be the error information given by the feed-back circuit. Figure 3.20 shows the profile of speed and current during seek. Figure 3.21 shows the waveform of -FNPOS and Error signal.

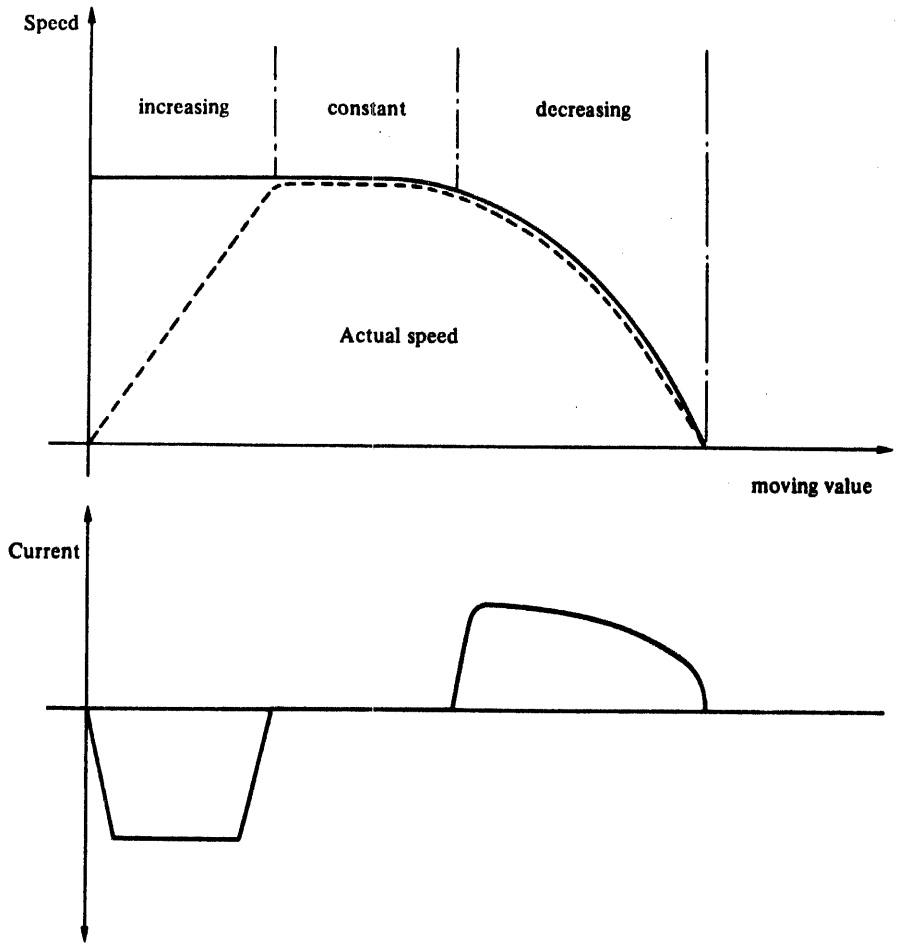


Figure 3.20 Seek Current

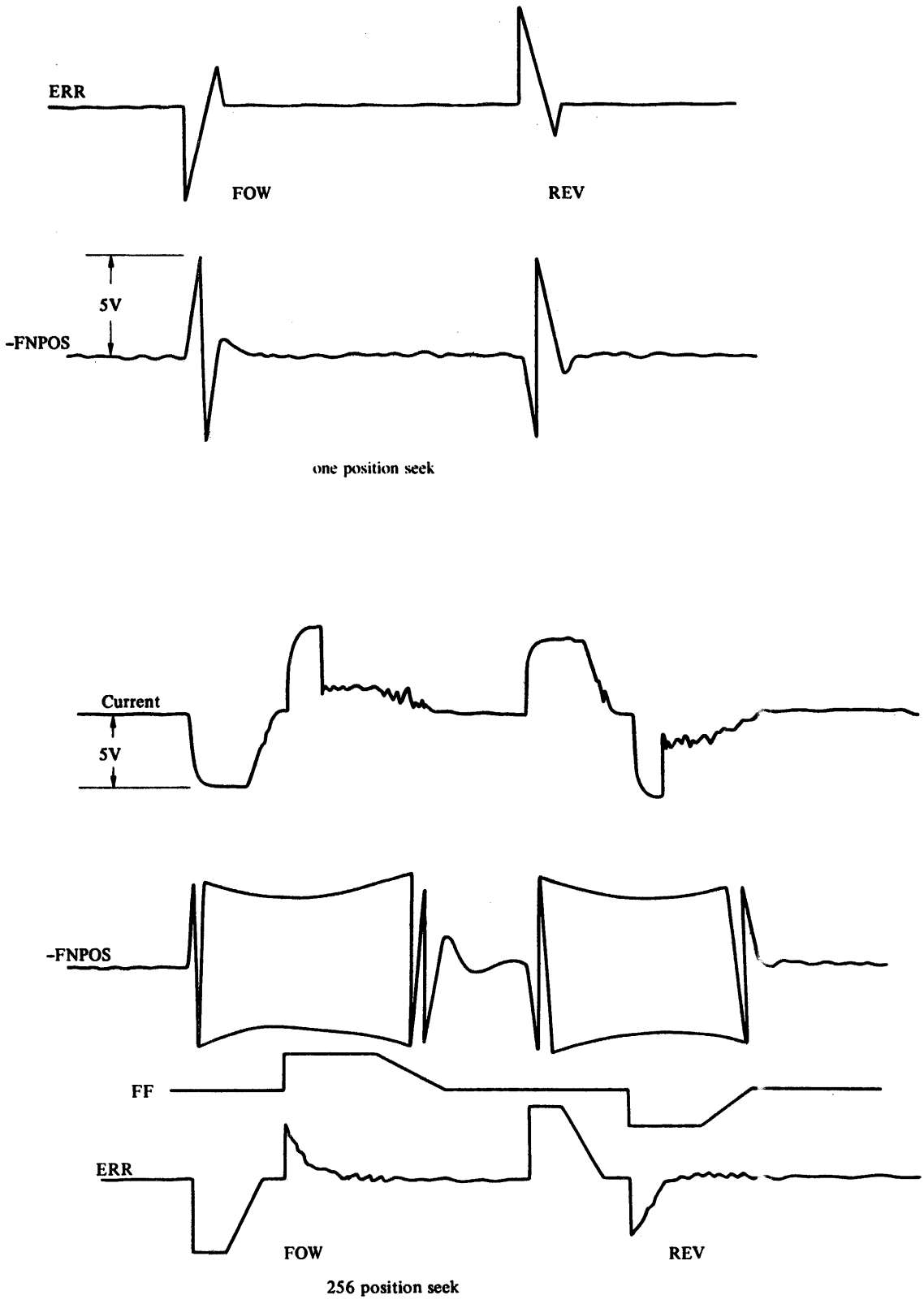


Figure 3.21 Waveforms During Seek

3.5.7 Servo demodulation circuit

As mentioned in subsection 3.4.1, the two-phase information written on the lowest order disk is read by the servo head and is sent to the AGC Amp. This Amp supplies a constant output even if the input is changed. This output is sent to a low-pass filter (LPF). The LPF will remove high frequency noise. This output is converted into Servo (CNH2-7) signal having a 10 Vp-p.

The servo signal is converted into a pulse by the level slice comparator. The trailing edge of the sliced pulse triggers a one-shot 100 ms pulse and another trigger one-shot (550 ms window) for separating servo pulses. Servo pulse (SVP) is generated by these two signals. SVP is a pulse having a four byte period. Noise on SVP is removed by gating with a 5us one-shot. SVP is triggered by a 3us one-shot. CPL signal is sent to a PLO (phase locked oscillator). CPL signal is phase-compared with CT7 signal, the resulting signal is converted into a voltage in the charge pump circuit (4044), and sent to the VCO (voltage control oscillator) through a filter. Clock signal PLO1F from VCO is a one bit-cell clock synchronized with servo pulse (SVP). PLO1F clock is sent to the timing counter in LSI MB15238.

The timing counter generates the following signals using PLO1F signal and the signal generated by dividing PLO1F signal.

- *GT1, *GT2, *GT3, *GT4 - necessary for generation of peak holding servo information
- *CT15 - initial setting of dividing counter
- phase comparing with SVP

Servo signal is also sent to the peak hold circuit, and peaks of ODD1, EVEN1, ODD2, EVEN2 are held by *GT1 - GT4 signals. Output of each peak hold circuit is sent to the summing amplifier and two differential amplifiers through the buffer amplifier, and generates AGC voltage and two-phase position signal, POSN (Position Normal) and POSQ (Position Quadruture). Figure 3.23 shows the timing chart of the PLO circuit and the peak hold circuit. Figure 3.24 shows the timing chart of the fine position generation.

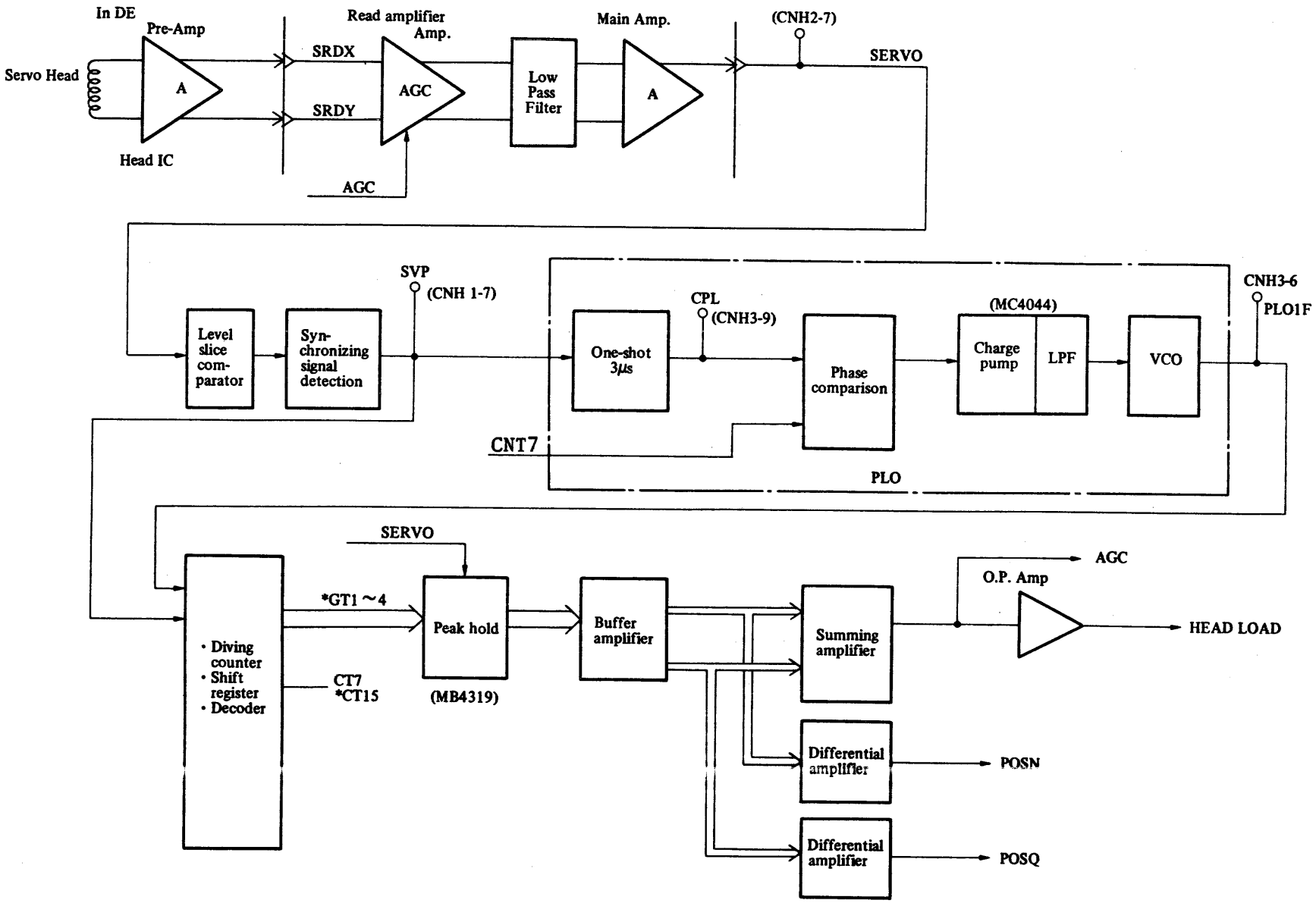


Figure 3.22 Demodulation Circuit

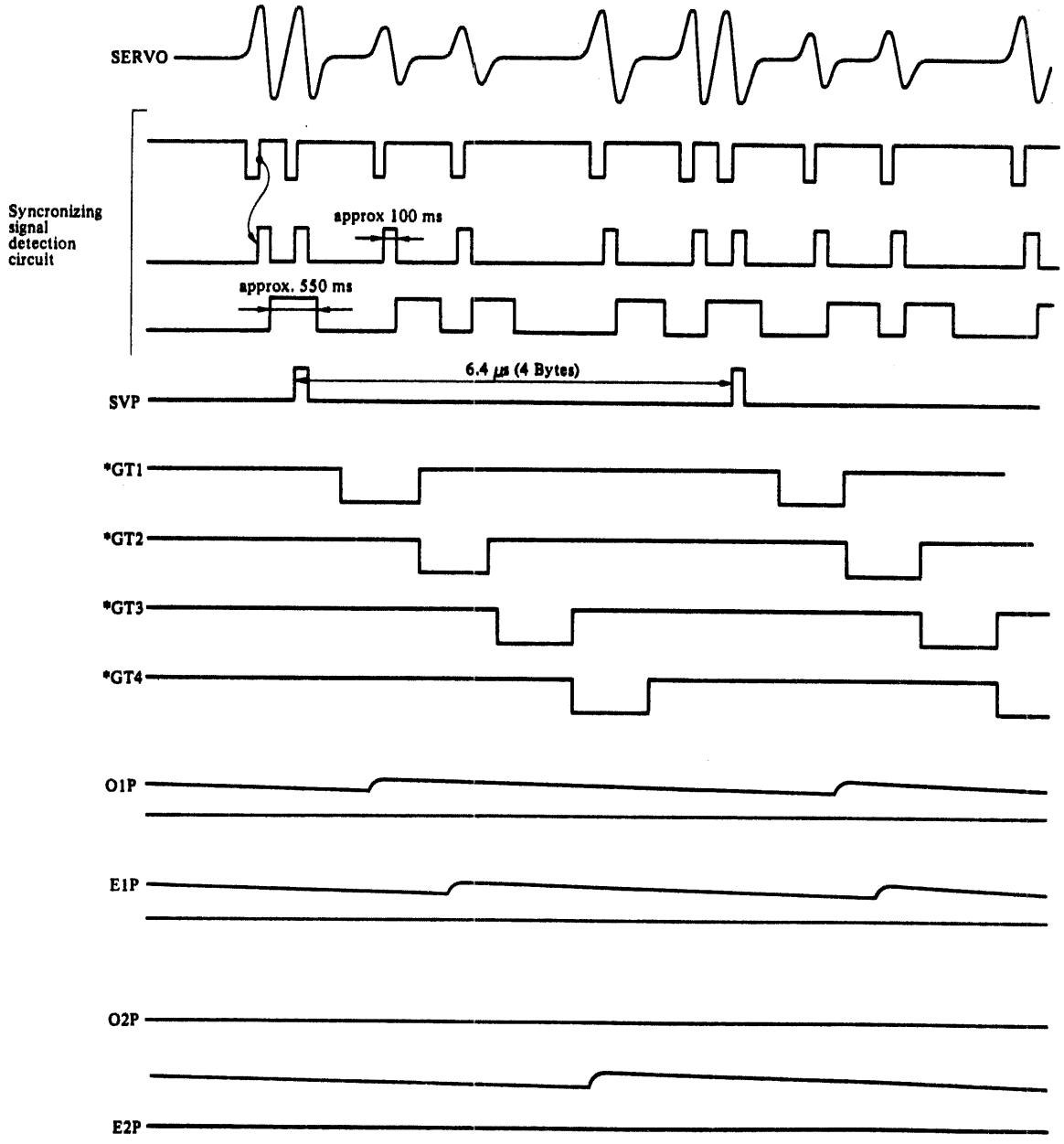


Figure 3.23 PLO/Peak Hold Timing

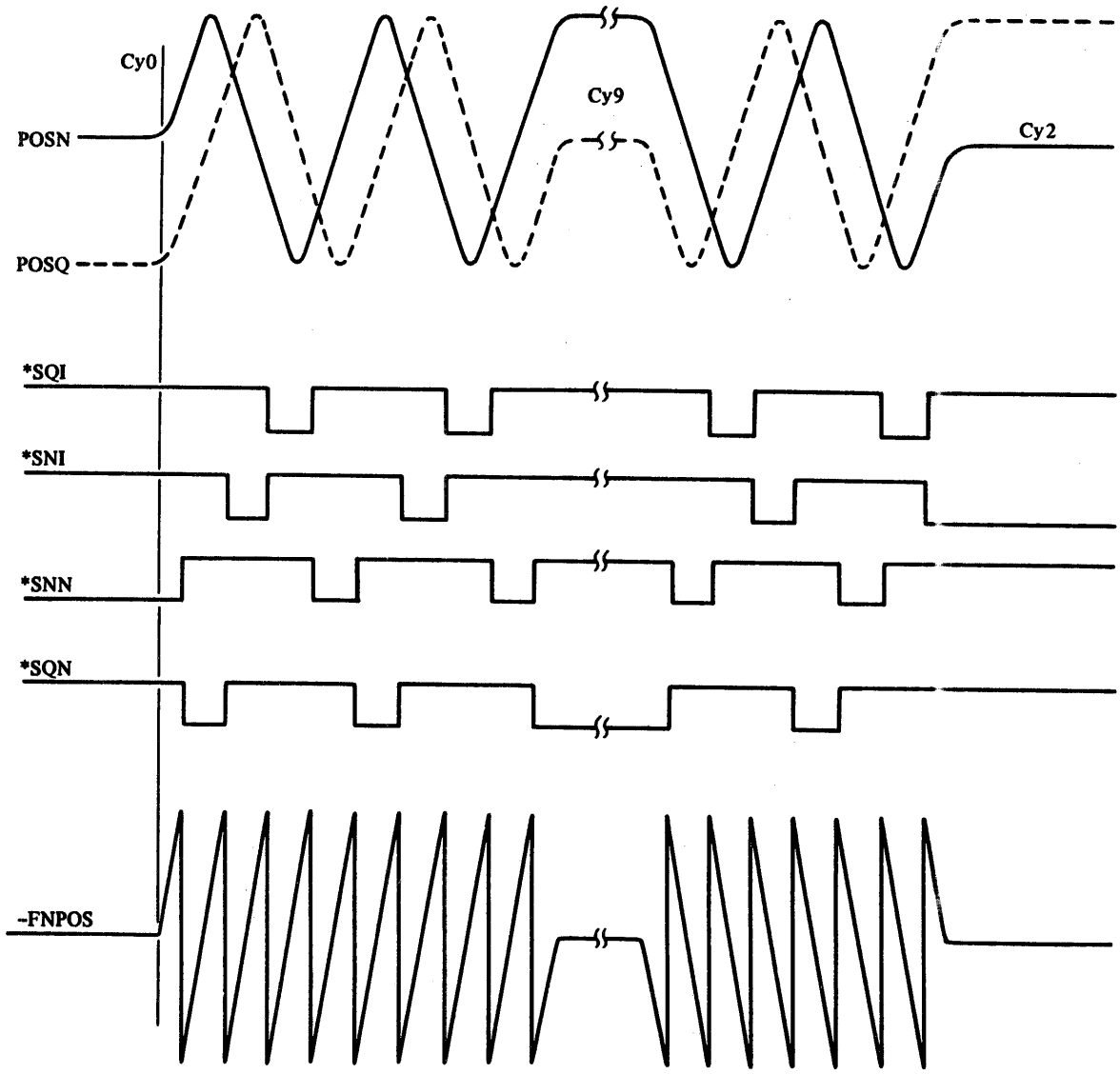


Figure 3.24 Fine Position Generation

3.5.8 Fault detection during seek

(1) VCMHT (VCM heat detection circuit); (Fault code 02)

If abnormal current flows into the VCM, the VCM heat detection circuit detects it and sends VCMHT signal to the MPU.

(2) Seek timeout (Fault code 09)

The timer/counter in the MPU is set to 0.8 sec before starting a seek. During this time (0.8 sec), if seek is not completed, internal interruption of MPU occurs and flow shifts from the seek operation routine to the time over routine.

(3) Over-shoot check (Fault code 0C)

After a seek, overshoot is checked. This is detected from difference between the current position and the target position.

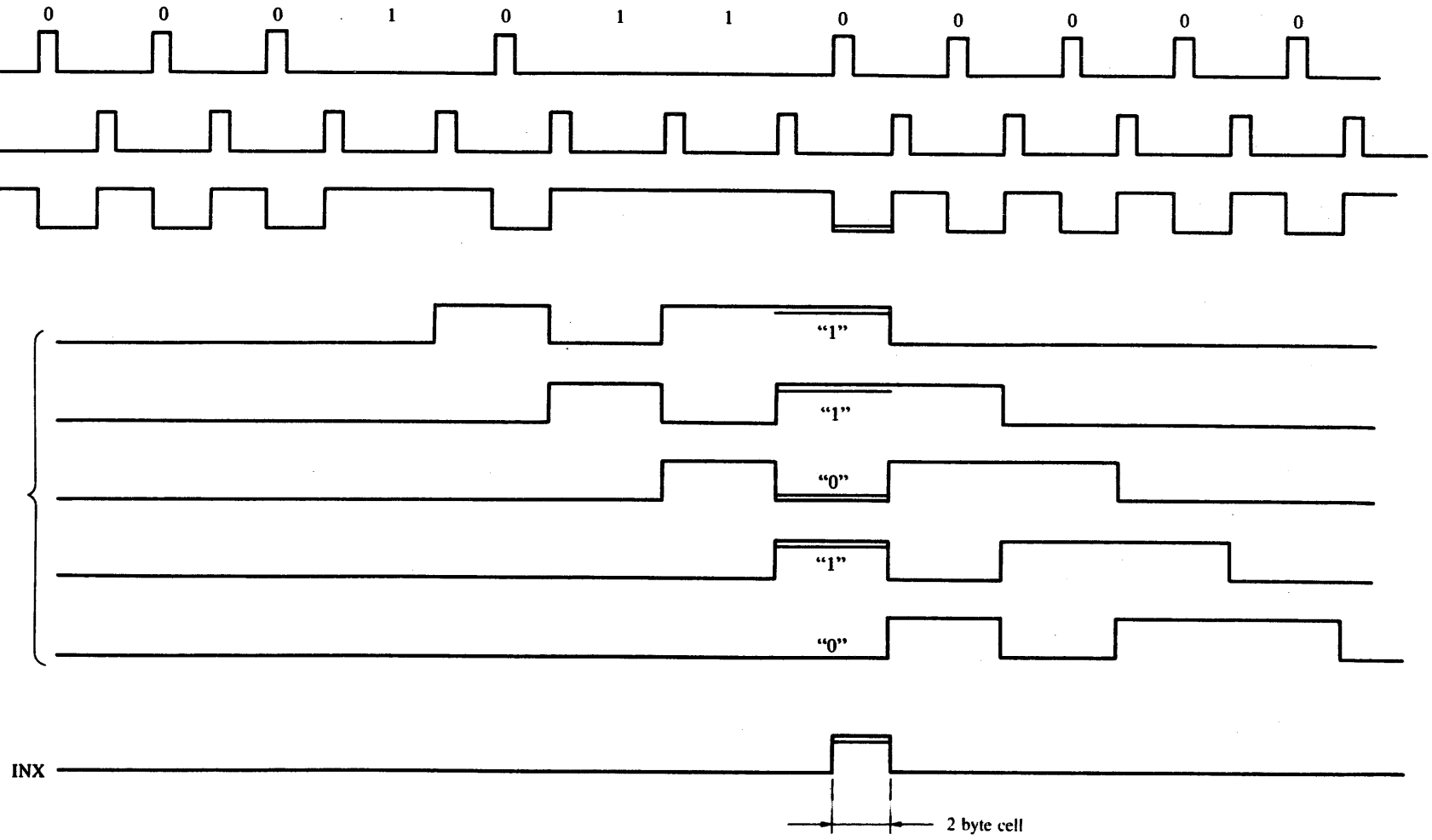
(4) Guard band detection (Fault code 0A/0B)

This fault indicates that guard band (IGB1, 0GB) is detected during seek operation. It is also reported when guard band is detected during track following (LNMD).

Each fault is coded during sequence, and is indicated by FLMP 0 - 3.

3.5.9 Index, guard band detection circuit

As mentioned in the servo track format section, the index bit pattern, including the missing index pulse, is in the servo pattern. Index, IGB1, IGB2 and 0GB are detected by combining the index bit pattern and the normal bit pattern. The pattern detection is performed by sending PL0L signal. It is reset by SVP signal and set by CNT7 signal, through a shift register in MB15238 using the servo pulse (SVP) signal that is missing in the index bit pattern. Figure 3.25 shows the index detection timing.
In case of IGB1, IGB2 and 0GB, the pattern occurs every 260 bytes. If the servo head is positioned in the guard band area, the guard band signal becomes a continous signal because if the guard band pulse is inserted within 272 bytes again, guard band signal is kept in MB15238.



B03P-4805-0008A...01.1

Figure 3.25 Index Signal Detection Timing Chart

3.5.10 Read/Write circuit

(1) General description

The read/write circuit consists of the head IC section inside the DE, the head select circuit, the write circuit and the read circuit. Figure 3.26 shows the block diagram of the read/write circuit.

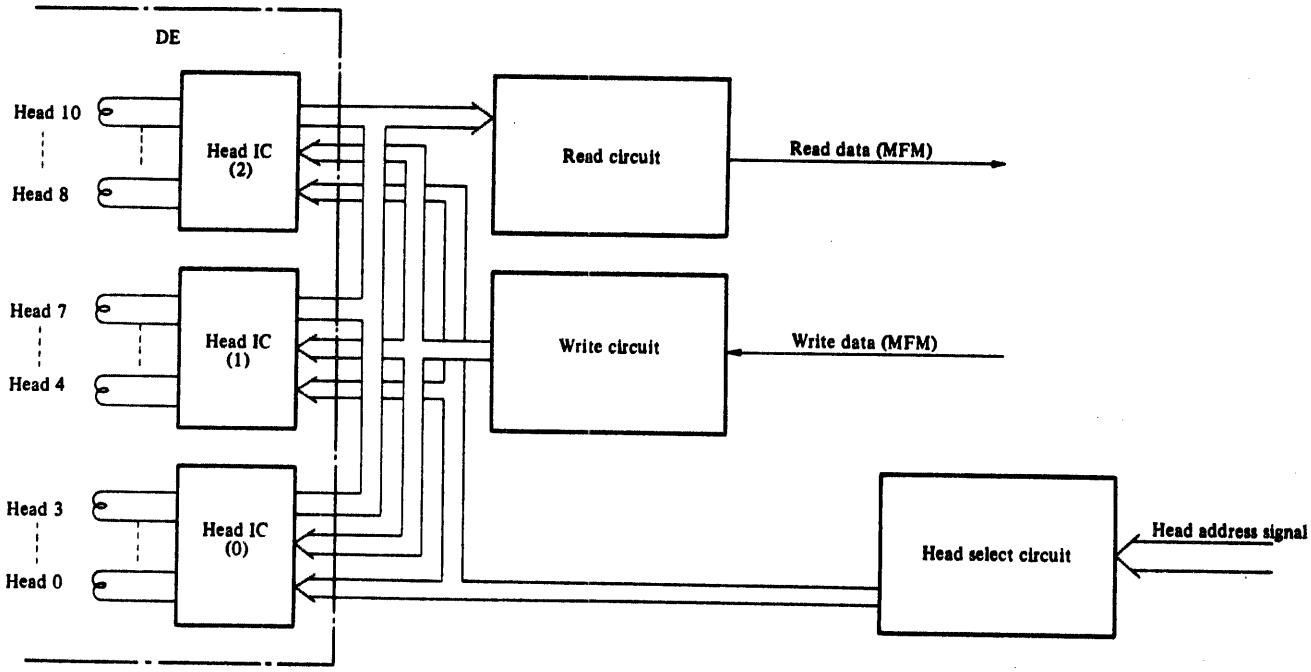


Figure 3.26 Read/Write Circuit Block Diagram

(2) Head IC section

The head IC section consists of 4 channel circuits, having the pre-amplifier and write amplifier. Each channel is connected to a data head. M2241AS, M2242AS and M2243AS have one, two and three head ICs inside the DE, respectively.

(3) Head select circuit

This circuit selects one head to record/read data by decoding Head Select 0 - 3 from the controller. This circuit further selects a head IC and finally a specific head.

(4) Write circuit

Figure 3.27 shows the block diagram of the write circuit.

a. Write amplifier

This is a current source detection circuit that determines the write current value of the head. This circuit is set on/off with write command signal (Write Gate) from the controller. The current value is changed according to the cylinder address of the head to control the optimum current to the head. If an error is detected in the WRITE FAULT of POWER LOSS detection circuit, the current source is cut off unconditionally.

b. Write driver

Write data received from the controller consists of write data pulses modulated to MFM. The write driver receives current from the write amplifier and controls the current to be sent to the data head according to the WRITE DATA PULSE.

c. WRITE FAULT detection circuit

This circuit detects write faults during the write operation. A fault will set the Fault Latch and send Write Fault to the controller in the following cases.

(a) When write current is not supplied to the head.

(b) When a non-select or multiselect state occurs in heads.

(c) When Write Gate is received in one of the following states.

- Not Ready state
- Before seek complete is set

(d) When the DC voltage is abnormal

(e) When an Off-track condition occurs.

d. POWER LOSS detection circuit

When the power is switched on/off or a power hit occurs, abnormal current may flow in the head because of a disturbance of the logic circuit, resulting in destruction of data on the disk. Therefore, the POWER LOSS detection circuit monitors the DC voltage level. The voltage clamps the write amplifier current source before the logic circuit is disturbed to protect the head from abnormal current.

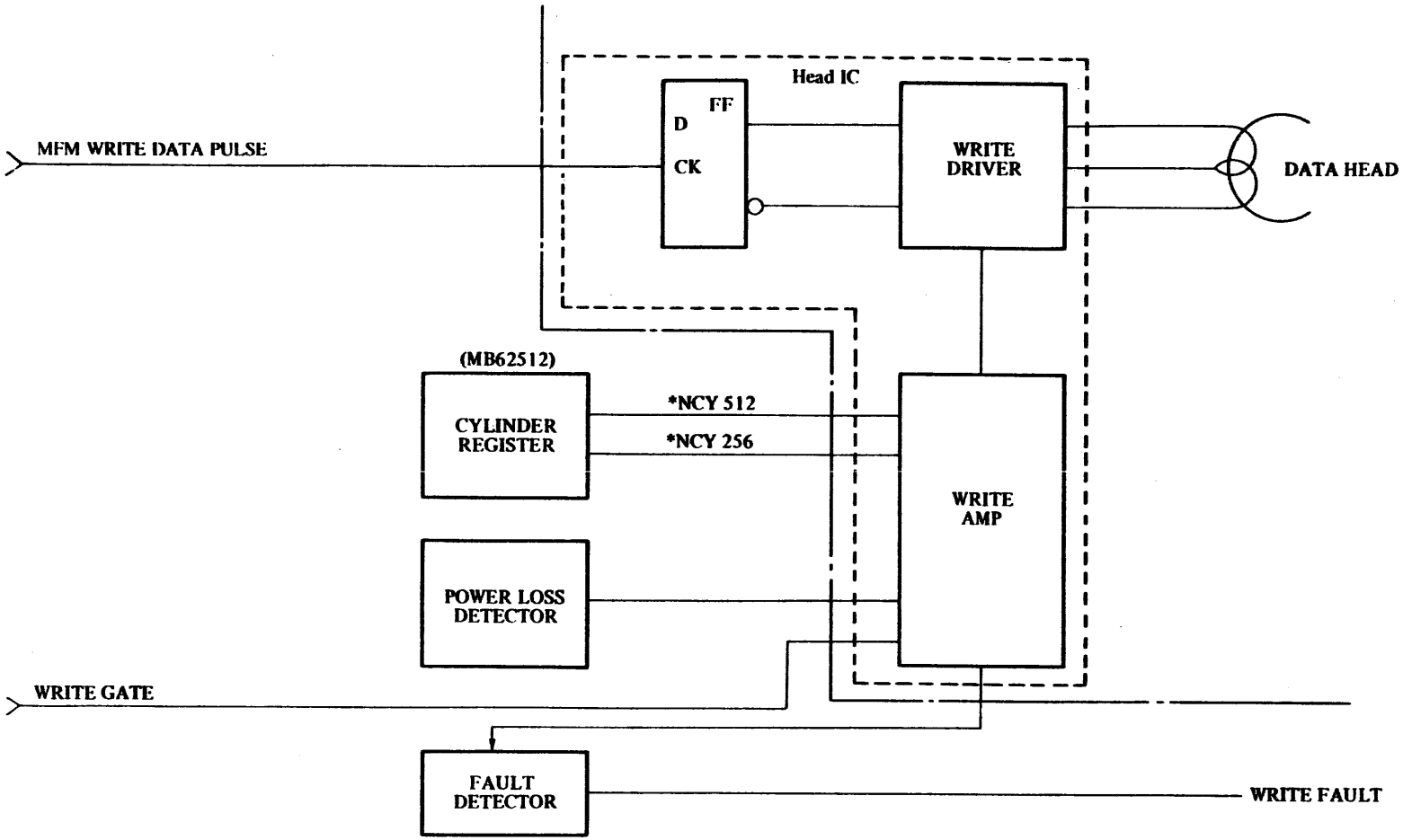


Figure 3.27 Write Circuit Block Diagram

(5) Read circuit

Figure 3.28 shows a block diagram of the read circuit and Figure 3.29 shows its waveforms.

a. Pre-amplifier

This is included within the head IC. Read signal generated by flux reversals on a disk and detected head output signal are input to the pre-amplifier, where they are amplified approximately 100 times.

b. Filters I and II

These filters eliminate high-frequency noise from read signals amplified by the pre-amplifier and main amplifier. The filter characteristics are changed according to the cylinder address of the head to compensate for the difference of head output signal characteristics between outer and inner cylinders.

c. Differentiation circuit

The peak position of read signal output from the pre-amplifier indicates the flux reverse point. This circuit, including CR, converts flux points to zero-cross points.

d. Main amplifier

This circuit amplifies signals differentiated by the differentiation circuit approximately 200 times.

e. Pulse shaper

This circuit detects zero-cross points of the differentiated waveform amplified by the main amplifier, then converts them to TTL level.

f. Shoulder noise elimination circuit

A read waveform sent from the head has shoulders shown in Figure 3.29. Differentiation of this waveform shows that the shoulders are close to the zero-cross line. External noise may add noise pulses to pulse shaper outputs.

The shoulder noise elimination circuit selects signal and noise pulses according to the pulse widths, and eliminates pulses narrower than the specified pulse width as noise pulses.

g. Waveform shaping circuit

This circuit generates raw data having the specified pulse width from the leading and trailing edges of the shoulder noise elimination circuit outputs.

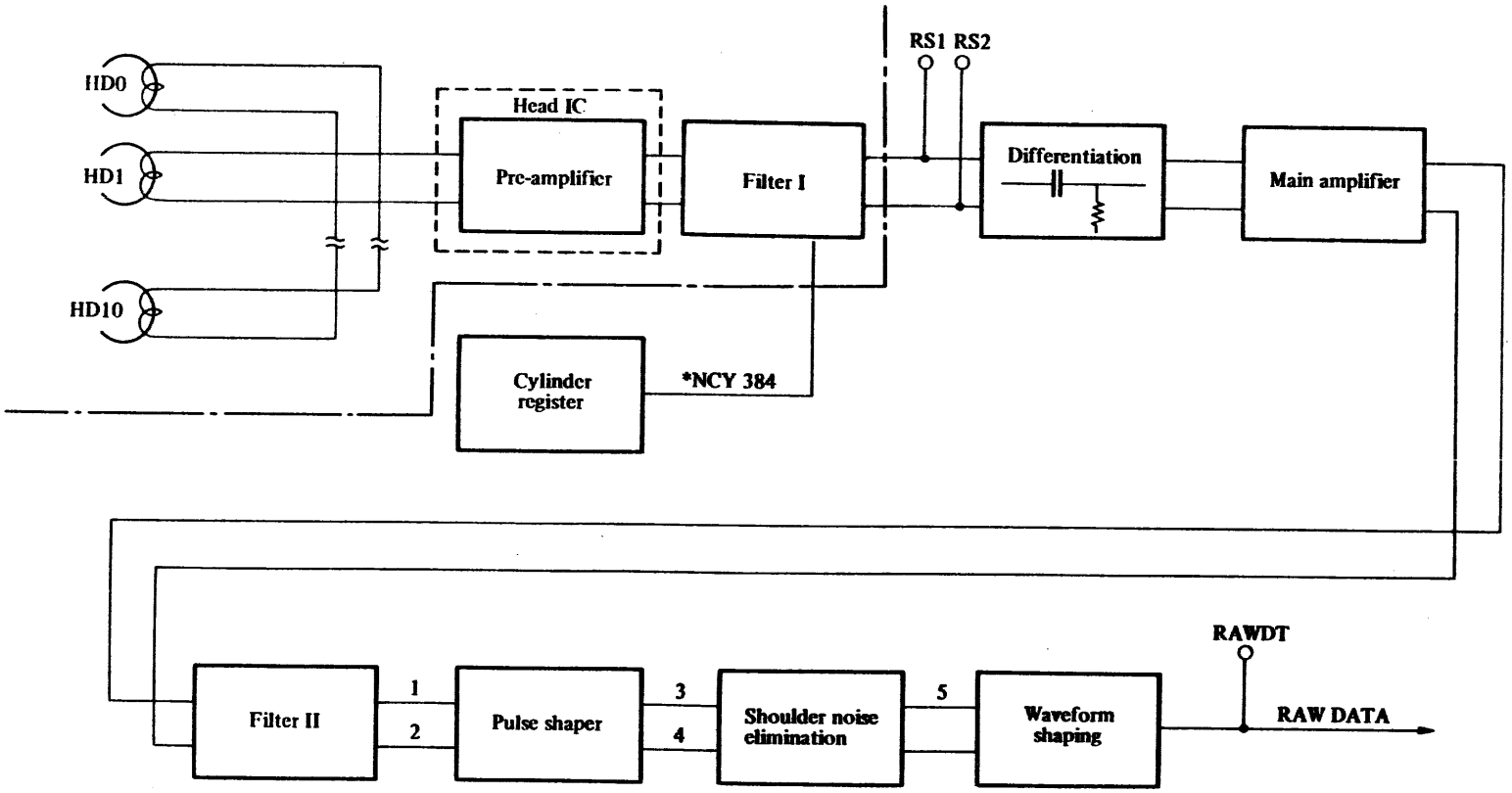


Figure 3.28 Read Circuit Block Diagram

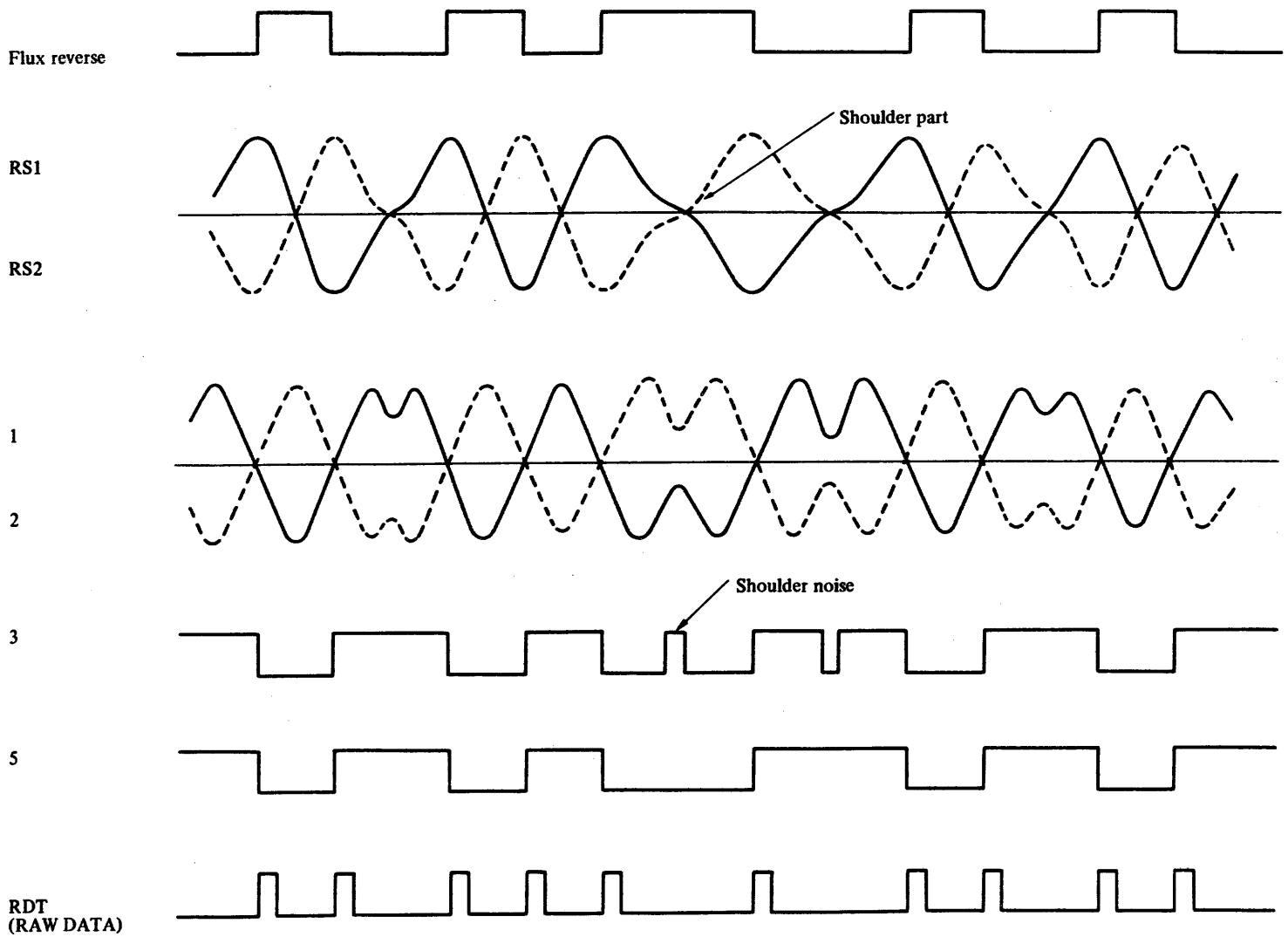


Figure 3.29 Read Circuit Waveforms

3.5.11 Fault detection

When a fault is detected, the fault is reported to the controller as Device Fault (FAULT), and detail status is coded by the MPU and displayed on LEDs for maintenance. Table 3.2 lists fault codes and description of fault.

Table 3.2 Fault status

Fault code	Description of Fault
01 (0001)	Abnormal rotation of DC spindle motor
02 (0010)	Abnormal current into VCM
03 (0011)	Initial seek time out
04 (0100)	Control check (write during seek)
05 (0101)	Write check 1 (abnormal voltage)
06 (0110)	Write check 2 (off track)
07 (0111)	Write check 3 (Write current abnormal)
08 (1000)	Write check 4 (multiselect)
09 (1001)	Seek time out
0A (1010)	Guard band during seek
0B (1011)	Guard band under linear mode
0C (1100)	Overshoot
0D (1101)	Abnormal address check
0E (1110)	Head is positioned outside of servo area
0F (1111)	Undefined

Note: A '1' in parentheses represents a light which is on. Fault lamp (FLMP) 0 is the LSB and FLMP 3 is the MSB.

3.5.12 -12V power generation

The −12 volts is derived from the +12 volts for servo control. This is accomplished by the DC-DC converter circuit in the power amplifier PCB (TVSM).

CHAPTER 4
TROUBLESHOOTING

4.1 General Description

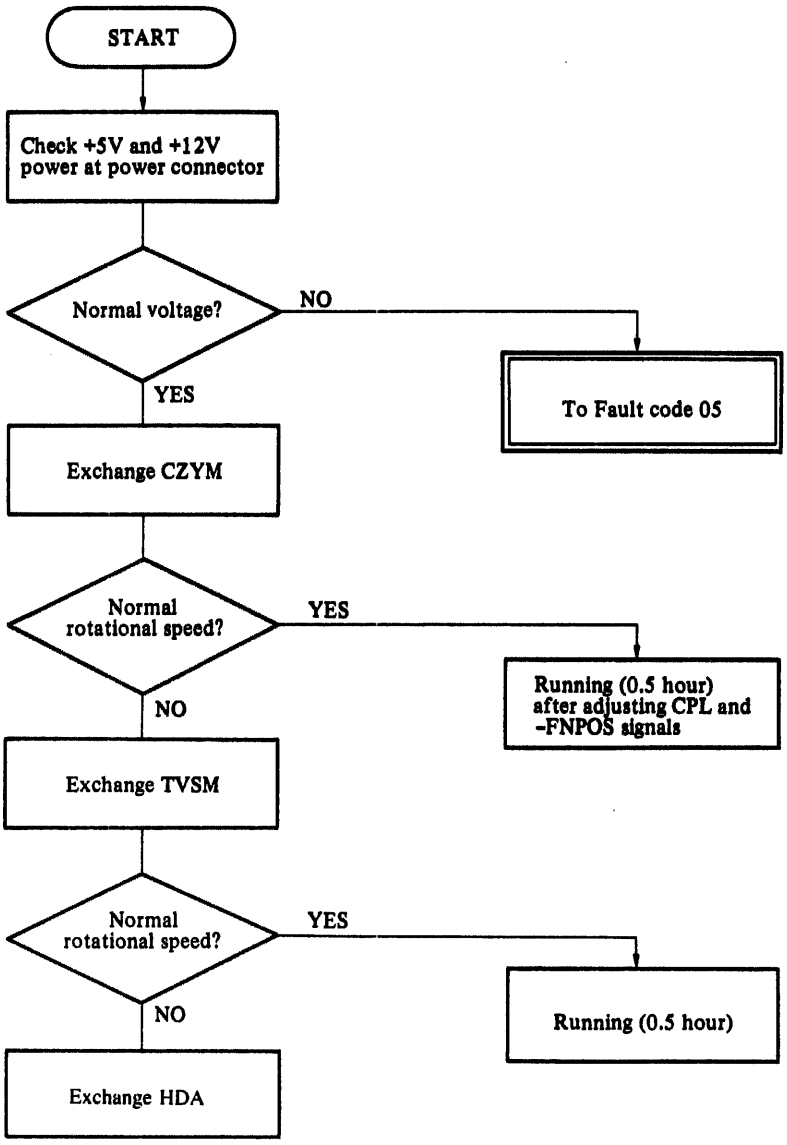
This chapter covers troubleshooting procedures for the M224XAS to locate problems in the PCBs and drive mechanisms. LEDs (Fault LEDs) on the PCB indicate any abnormal status, except data error during read operation.

4.2 Troubleshooting

Troubleshooting procedures for abnormal status indicated by LED's (Fault code 01 to 0E) and read errors are shown in this section by the use of a flowchart.

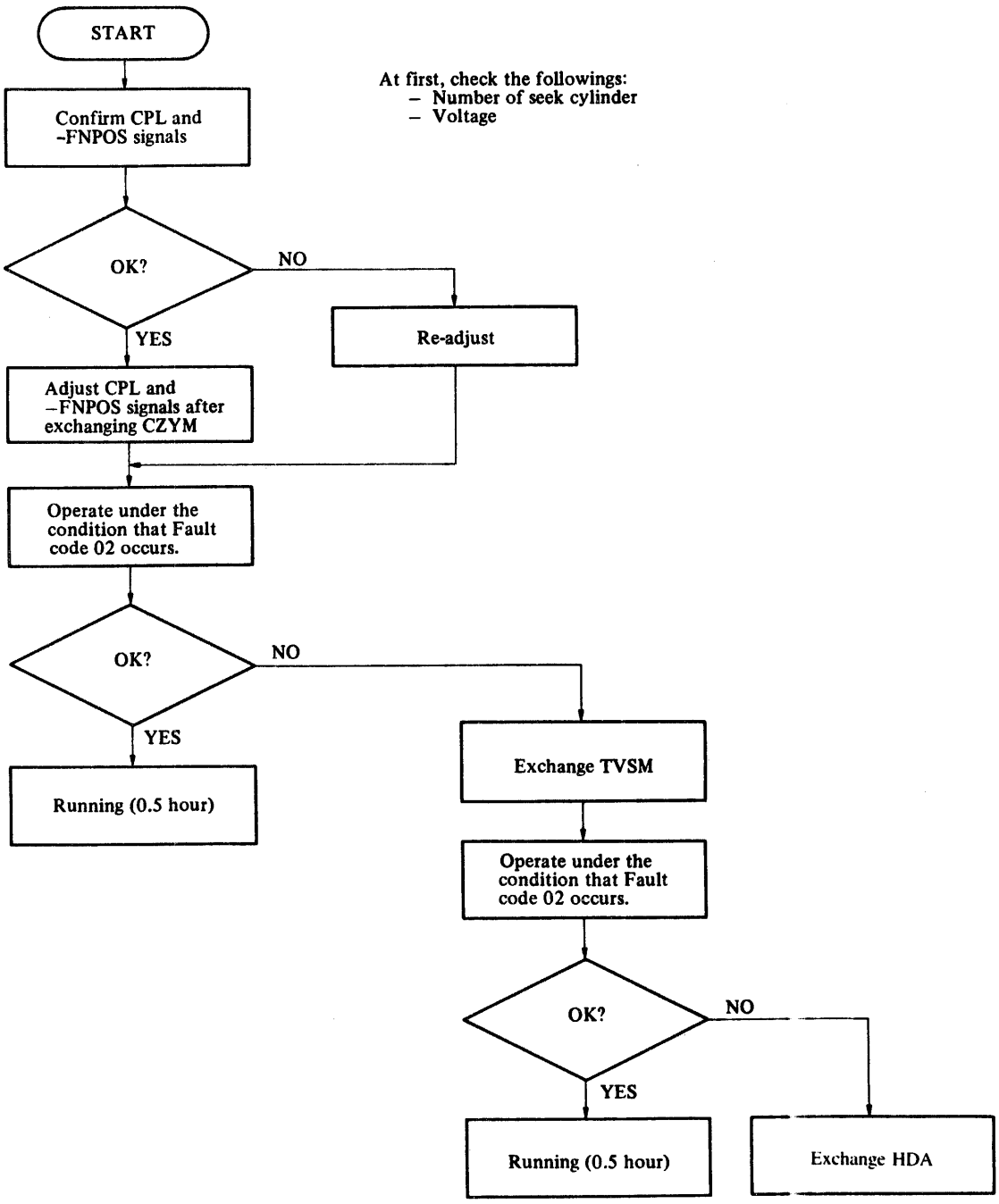
Fault Code 01 (0001)

Rotational speed of DC motor was less than 90% of standard speed, or DC motor did not rotate.



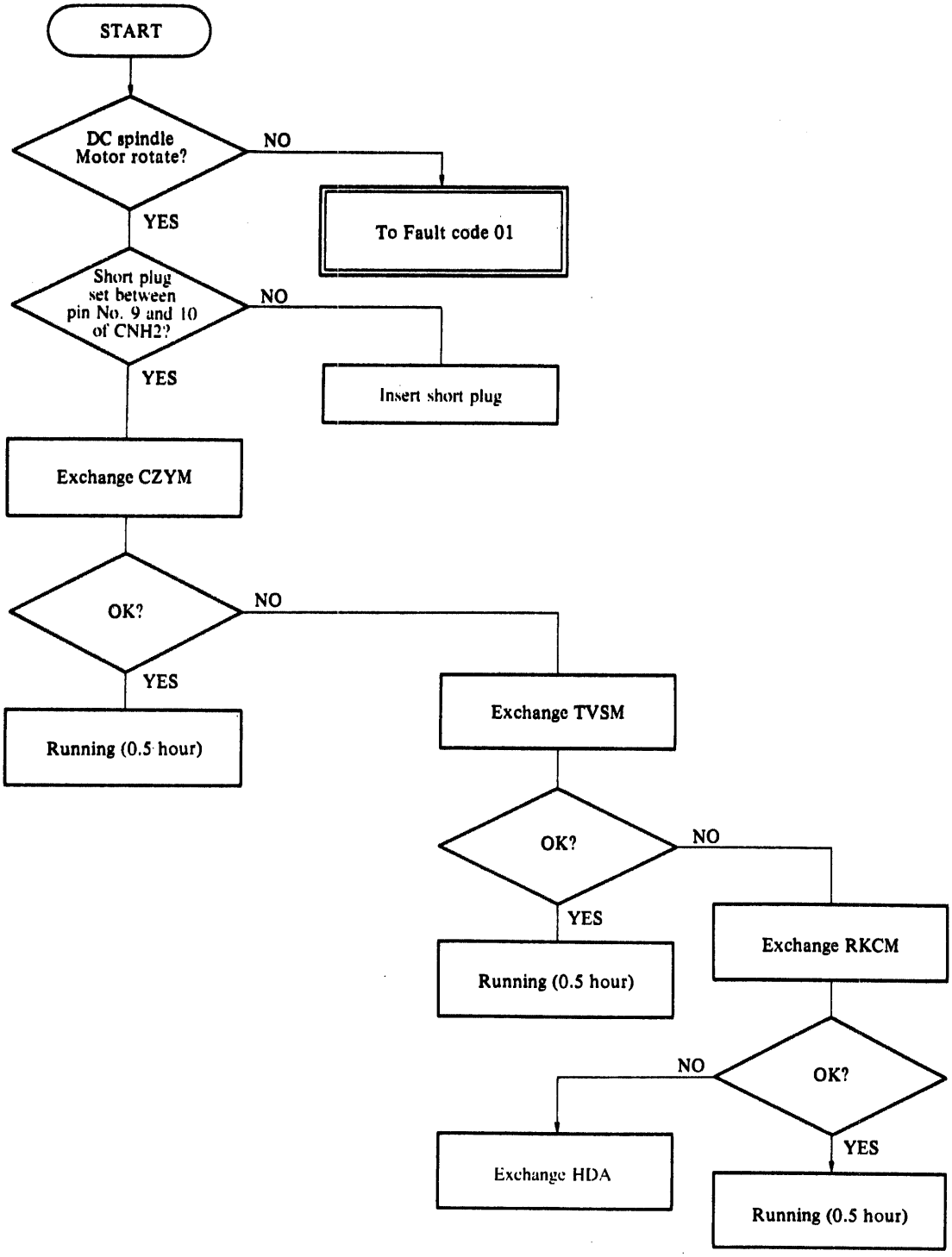
Fault Code 02 (0010)

Abnormal current flow to VCM (VCMHT).



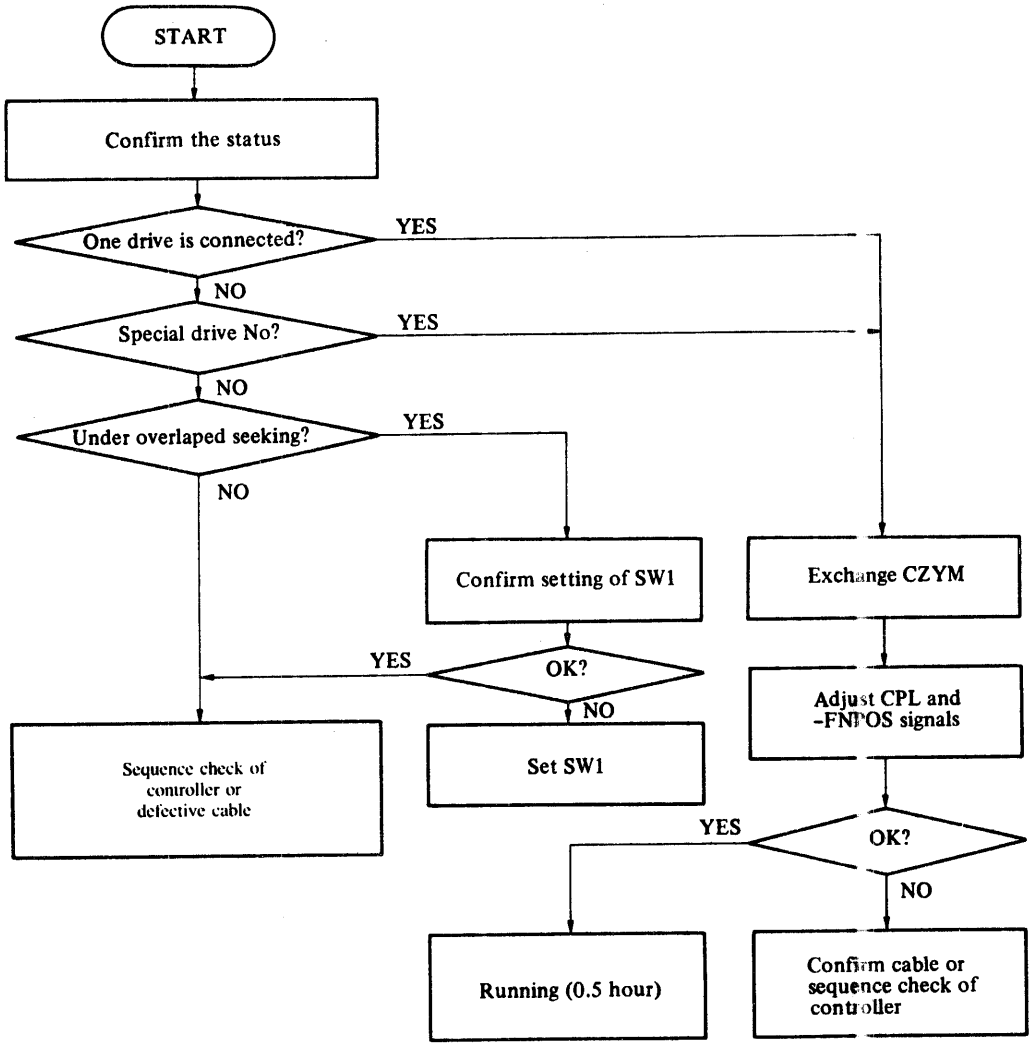
Fault Code 03 (0011)

Initial Seek Time-Out



Fault Code 04 (0100)

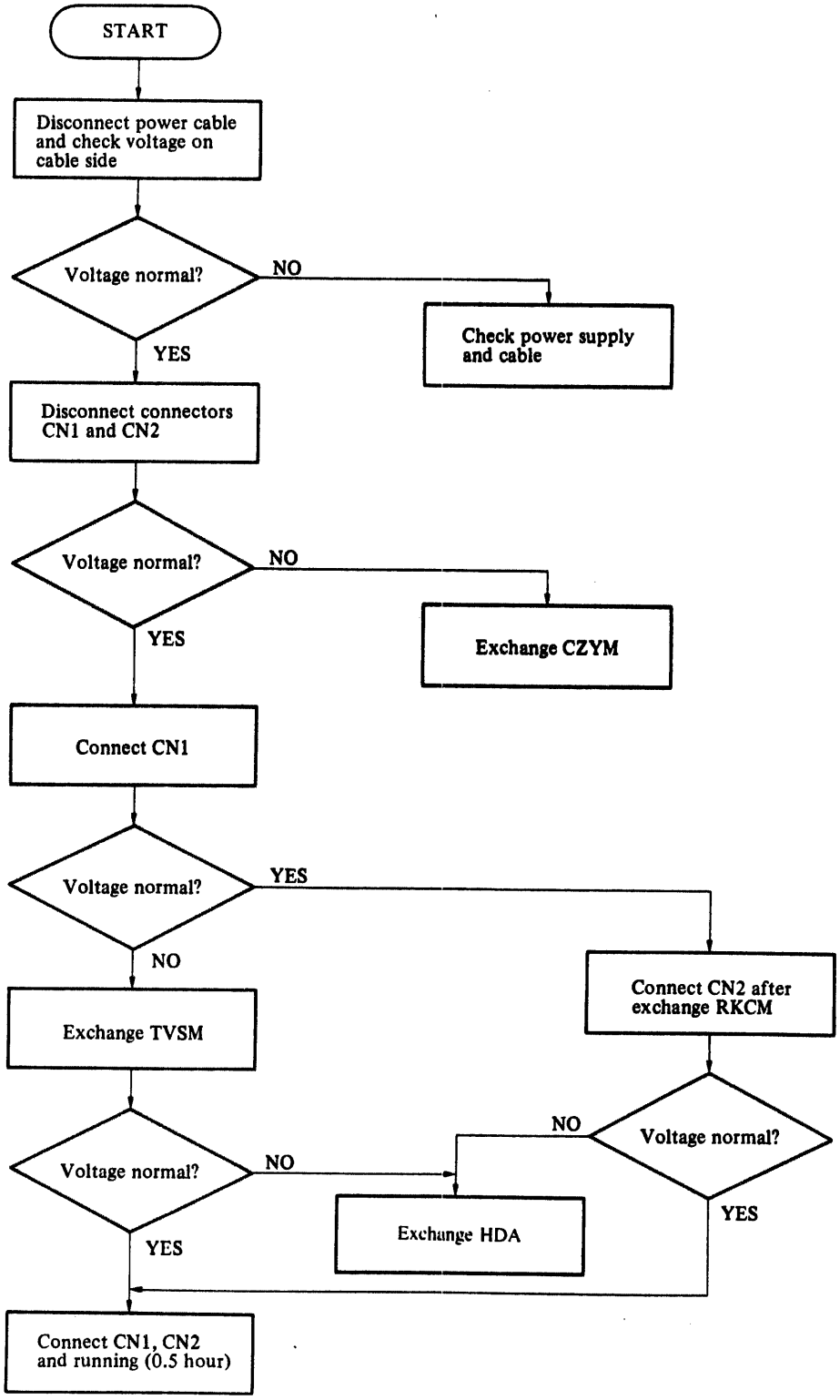
Write command issued during seek operation.



Note: Causes of this fault code are as follows.
- Abnormal sequence of controller
- Defective CZYM
- Defective interface cable

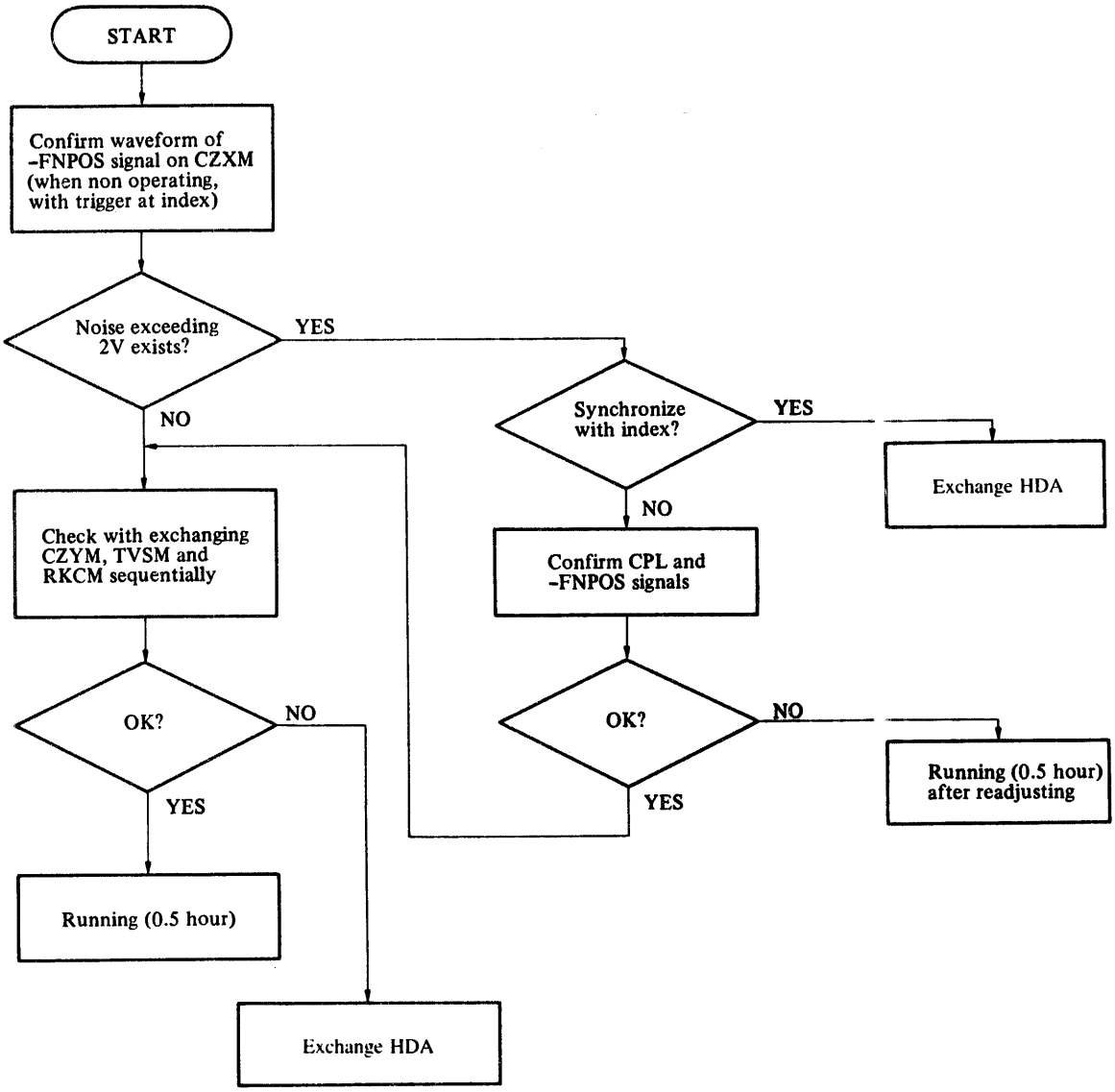
Fault Code 05 (0101)

Either +12V or +5V power is less than 80% of specified voltage during write operation.



Fault Code 06 (0110)

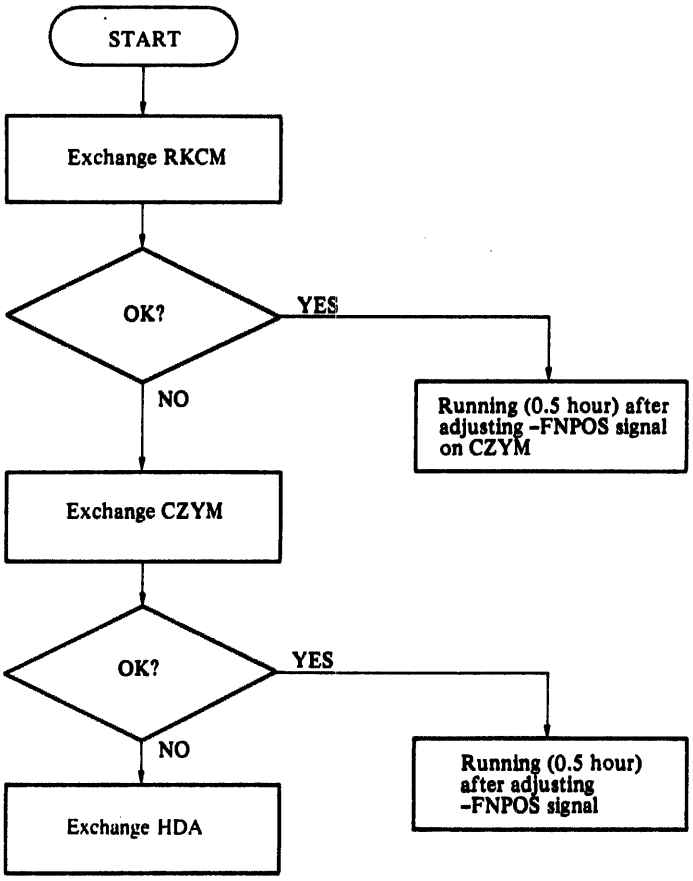
Off track occured during write operation.



Note: This fault may occur with excessive external shock or vibration.

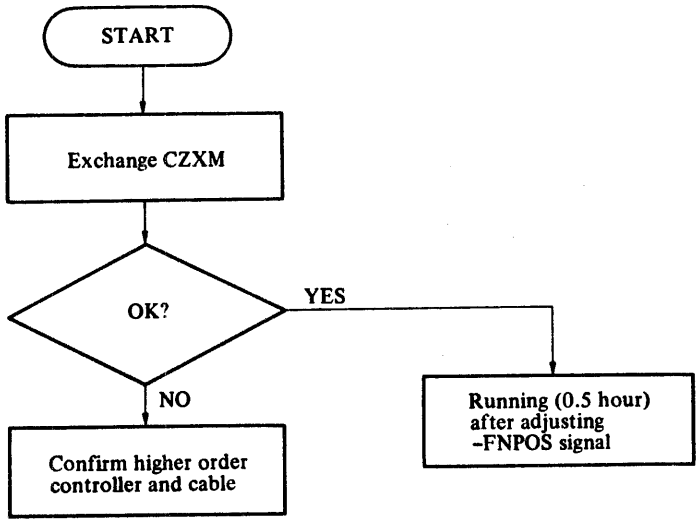
Fault Code 07 (0111)/08 (1000)

Write current was abnormal.
Two or more heads were selected during write operation.



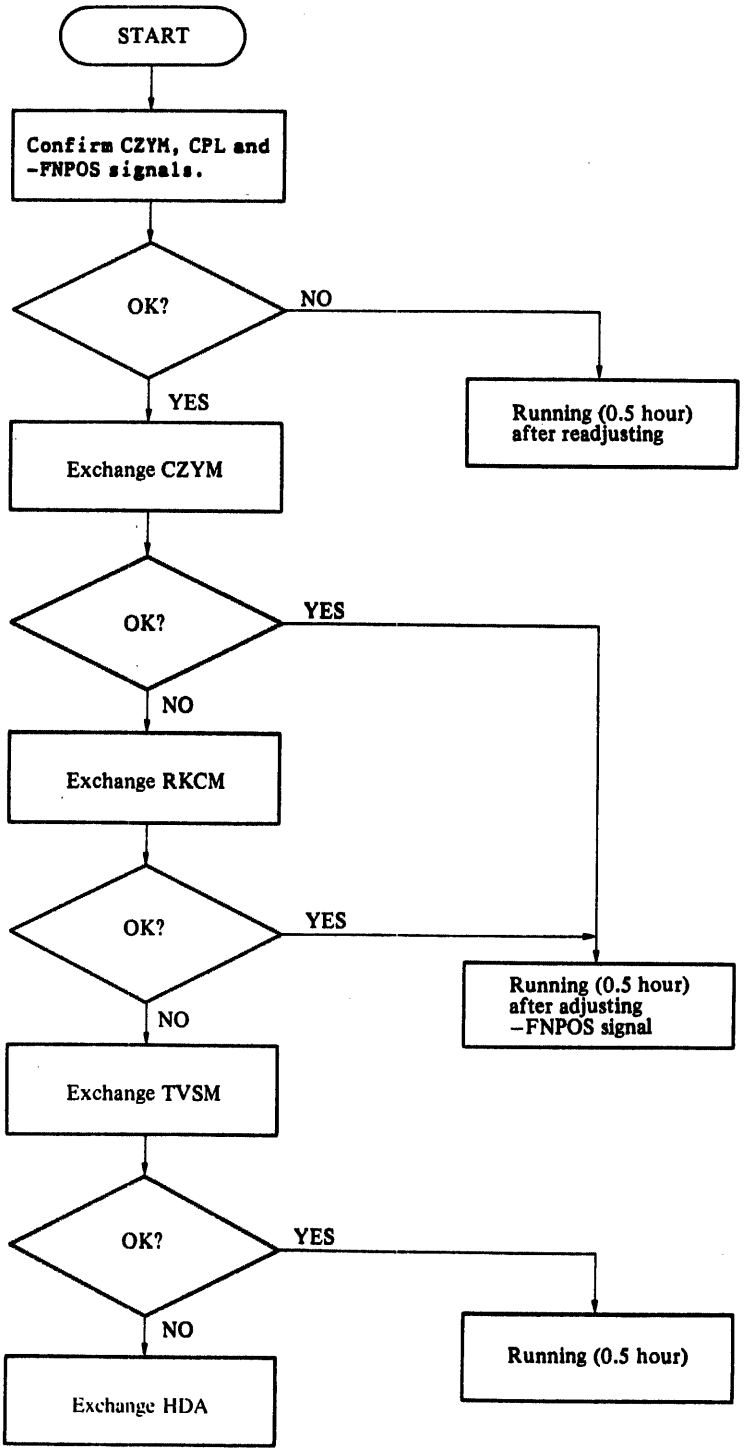
Fault Code 0D (1101)

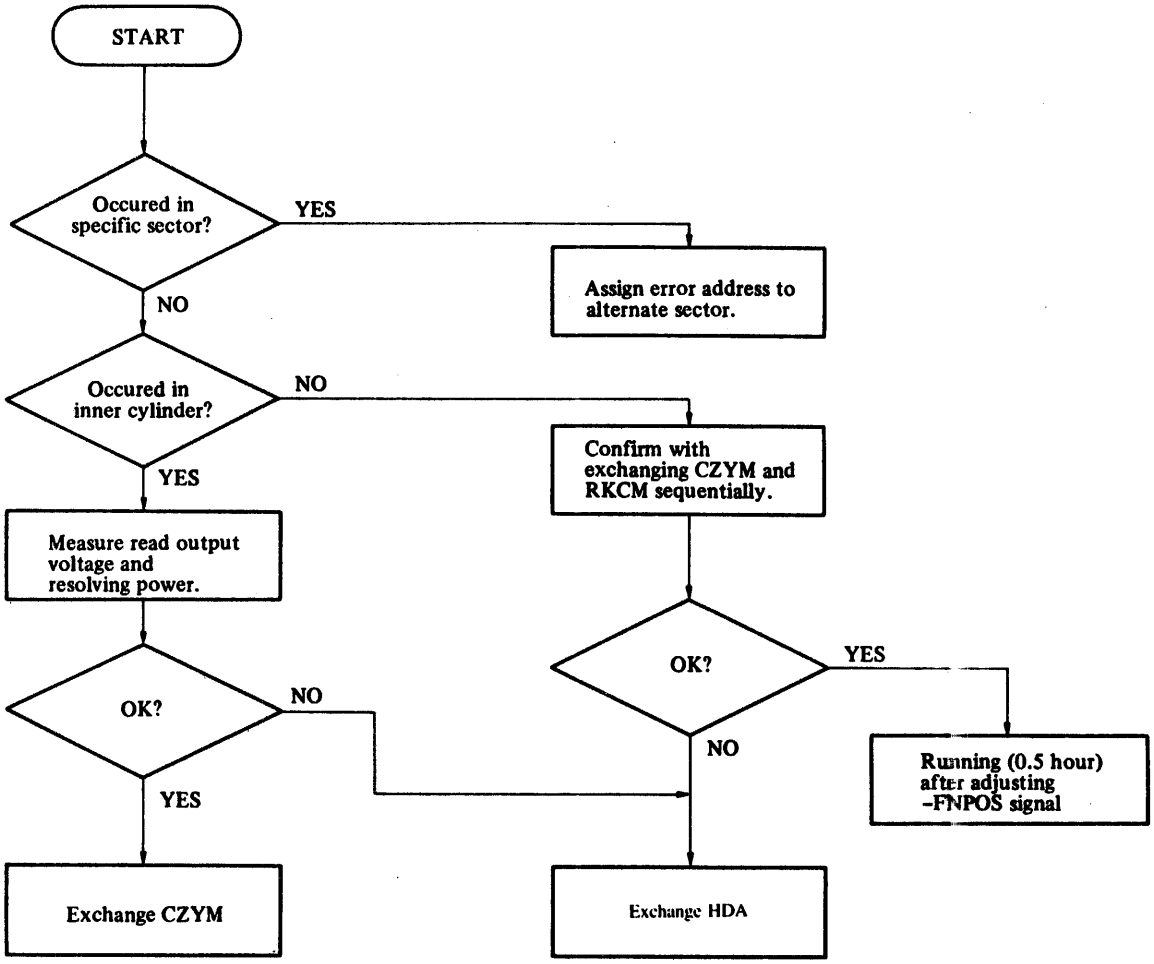
Seek command issued to cylinder other than cylinder 0 to 753.



Fault Code 09/0A/0B/0C/0E

Seek timeout error.	09
Guard band was detected during seek operation.	0A
Guard band was detected under linear mode.	0B
Over shoot check.	0C
After ready state, head load signal became false.	0E




START
Occured in specific sector?
YES
Assign error address to alternate sector.
NO
Occured in inner cylinder?
NO
Confirm with exchanging CZYM and RKCM sequentially.
YES
Measure read output voltage and resolving power.
OK?
YES
NO
Running (0.5 hour) after adjusting -FNPOS signal
OK?
NO
YES
Exchange CZYM
Exchange HDA

CHAPTER 5
MAINTENANCE

5.1 General Description

This chapter describes the maintenance procedure for the M224XAS. It consists of general information, preventive maintenance, adjustments and electrical verification.

5.2 General Information

5.2.1 Power on/off

(1) After a visual check of the drive, verify power by turning the drive ''ON'' and ''OFF''

(2) Following maintenance, confirm all PCB's are in proper location and secure.

5.2.2 Cables/Connectors

Do not remove or install any cables or connectors with power on.

If a cable has been installed or re-installed, verify that it is connected properly.

5.2.3 Parts Replacement

(1) Use a suitable tool for each part.

(2) Save all parts removed, such as screws, brackets, etc.

(3) Secure all parts after replacement.

5.2.4 Test/Check Out

(1) Run appropriate tests to verify operation.

(2) Record repair and test results.

5.3 Maintenance Tools and Equipment

Maintenance tools and equipment listed in the following table are for special use, for example trouble recovery, they are not required for routine maintenance.

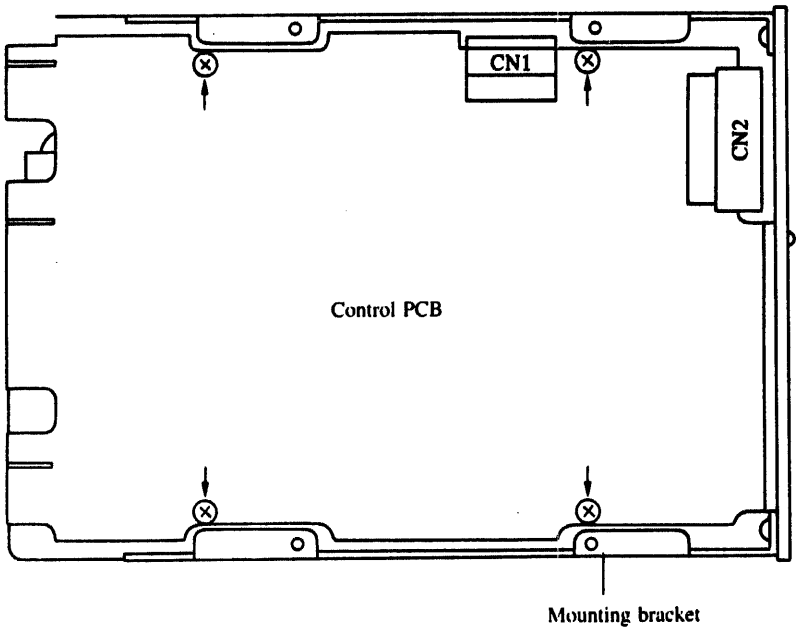
Description	Specification
Oscilloscope	Tektronix 475 or equivalent
Scope Probe (X 10)	Tektronix P6053B or equivalent
Digital multimeter	
Screwdriver for adjustment	
Screwdriver	Number 2 Phillips

5.4 Preventive Maintenance

Preventive maintenance is not required.

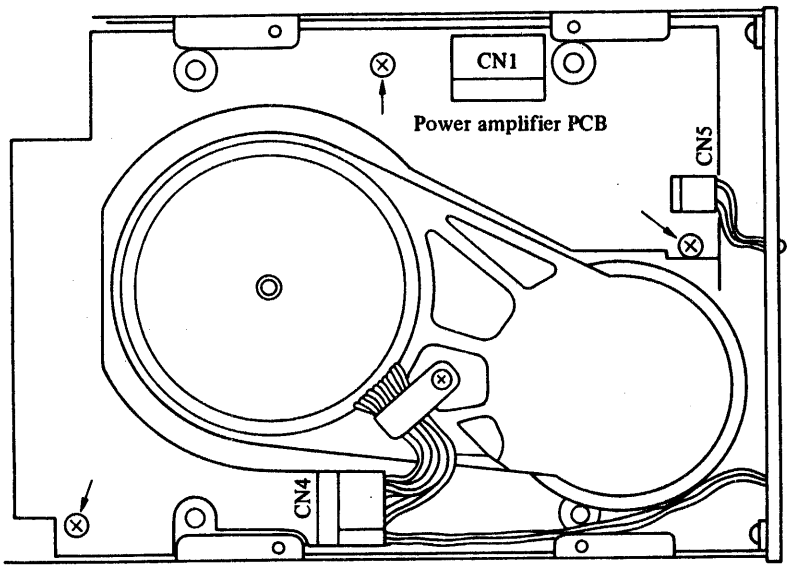
5.5 PCB Removal

(1) Control Y CZYM PCB



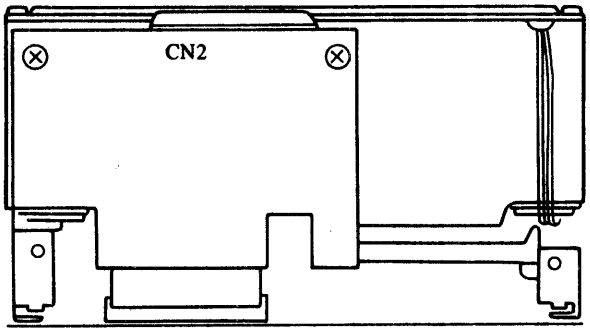
1. Remove 4-M3 screws
2. Disconnect CN1
3. Disconnect CN2
4. Remove PCB

(2) Power amplifiers TVSM PCB



1. Remove 3, M3 screws
2. Disconnect CN5 and CN1
3. Disconnect CN4 while lifting CN1 side of PCB
4. Remove PCB

(3) Read amplifier C RKCM PCB



(1) Remove front panel from mounting brackets.
(2) Remove 2, M3 screws
(3) Disconnect CN2 while lifting the side of the PCB opposite CN2. At this time, be careful not to break the flex cable/connector.
(4) Remove PCB.

5.6 Verification and Adjustment

5.6.1 Location of test points, adjustments and fault indicators.

Figure 6.1 shows the test points and adjustments on the control (CZYM) PCB.

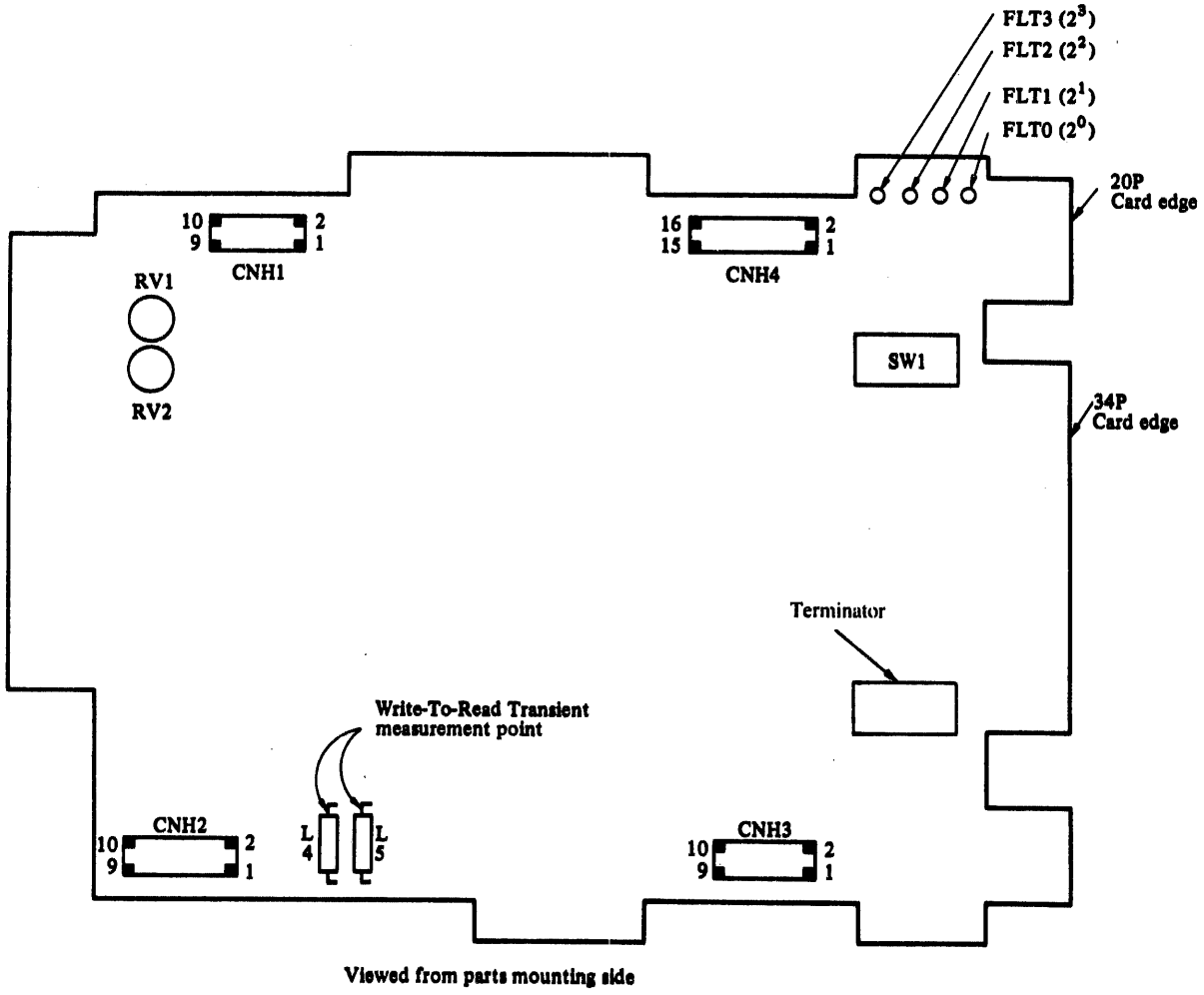


Figure 5.1 Location of Test Points and Adjustments

5.6.2 Signals on test points

(1) CNH1

10	9	8	7	6	5	4	3	2	1
OFF TRACK	+FNPOS	P2F	SVP	-FNPOS	N+Q>0	N>Q	PSQ	PSN	0V

(2) CNH2

10	8	6	4	2
PWDR	PWDR	SSG	CD1	RS1
9	7	5	3	1
PWDR	SERV0	5VA	RS2	0V

Note: Pin No. 09 and 10 must be shorted with the shorting plug.

(3) CNH3

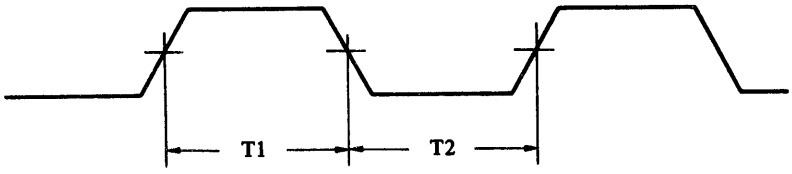
10	8	6	4	2
*DRLM	RRD	PLO1F	-	0V
9	7	5	3	1
CPL	-	WDP	-	+5V

(4) CNH4

16	14	12	10	8	6	4	2
DIAG1	DIAG2	WGT	FLT3	FLT1	-	* WGT	SKC
15	13	11	9	7	5	3	1
0V	-	WFALT	FLT2	FLT0	-	DIRCT	INDEX

5.6.3 Confirmation of P2F signal

Measure pin No. 8 of the test point CNH1, and confirm the following



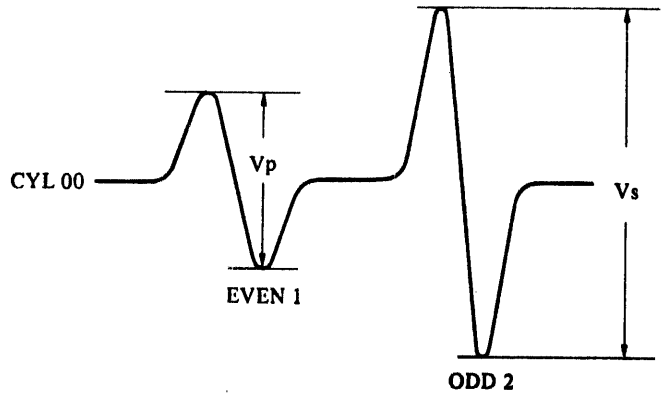
$$Rt = \frac{T_1}{T_1 + T_2} \times 100$$

$40 \leq R \leq 60$

$T_1 + T_2 = 100$ ns ± 0.5%

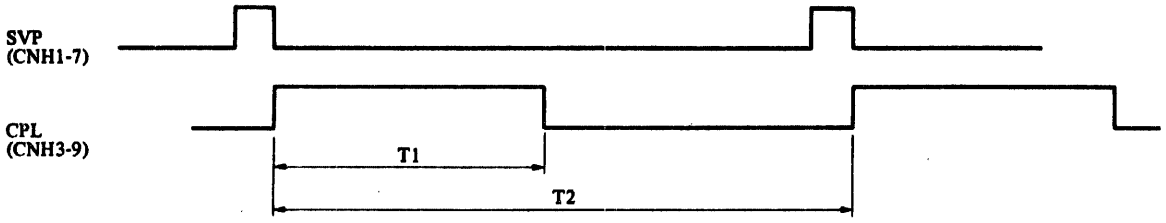
5.6.4 Confirmation of servo signal

Measure pin No. 7 of the test point CNH2, and confirm the following.



Vs = 8V ± 0.5V
Vp = 4V ± 0.5V

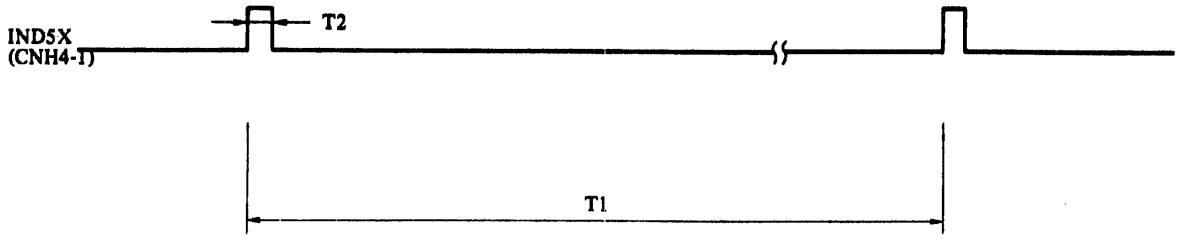
5.6.5 Confirmation of CPL signal



T_1 = 3.0 µs ± 0.1 µs
T_2 = 6.4 µs ± 0.2 µs

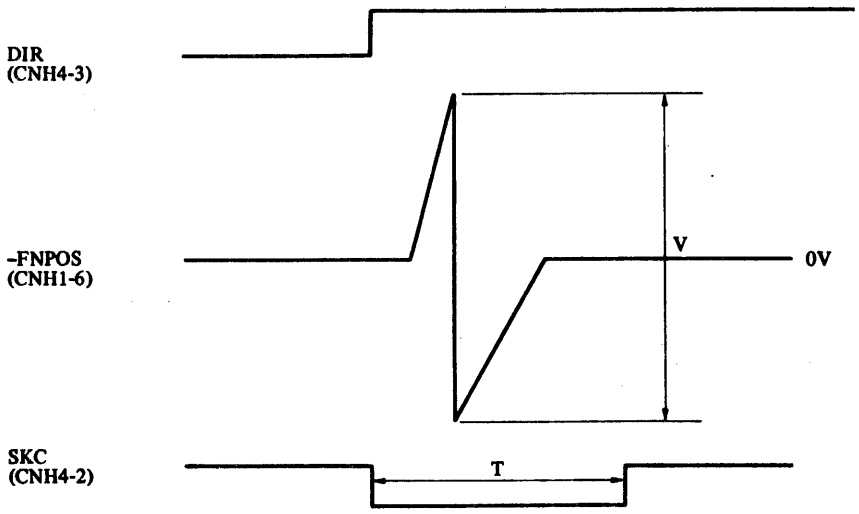
If T_1 is out of specification, adjust RV1.

5.6.6 Confirmation of Index signal



T_1 = 16.67 ms ± 1%
T_2 = 200 µs ± 50%

5.6.7 Confirmation of -FNPOS signal



V = 10V ± 0.5V
T ≦ 8 ms

Note: 1. Level of -FNPOS signal can be adjusted by RV2.
2. Adjustment and confirmation are performed by 1 track seek from cylinder 0 to cylinder 1.
3. When replacing HDA, CZYM or RKCM, -FNPOS signal must be adjusted.
4. Adjust the voltage to nominal value.

5.6.8 Confirmation of +12V power

Measure the lead of inductance L2 on CZYM and confirm the following specification is satisfied.

-12V ±10%

5.6.9 Confirmation of read output level

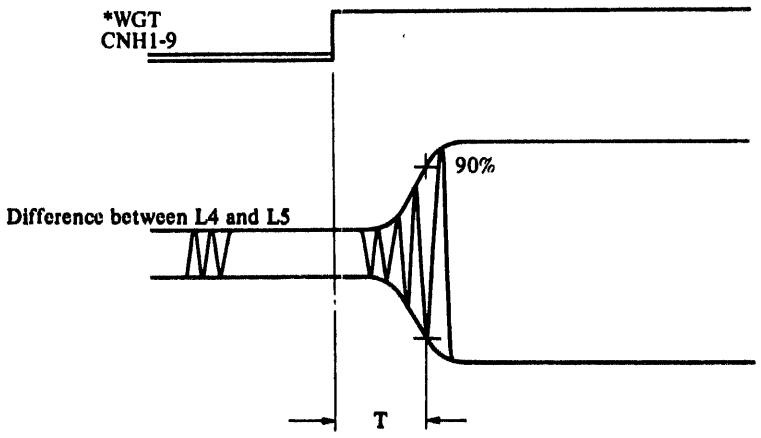
Observe differential at test points RS1 and RS2, output voltage V_1t and V_2t of 2t/1t, and resolving power (Res = V_1t/V_2t) must satisfy following specification.

(1) CYL 0 $V_1\tau \geqq 40$ mV Res ≧ 55%

(2) CYL 753 $V_2\tau \leqq 400$ mV Res ≦ 98%

5.6.10 Write-read transient

Transient is less than 8μs when writing the data with data write command.

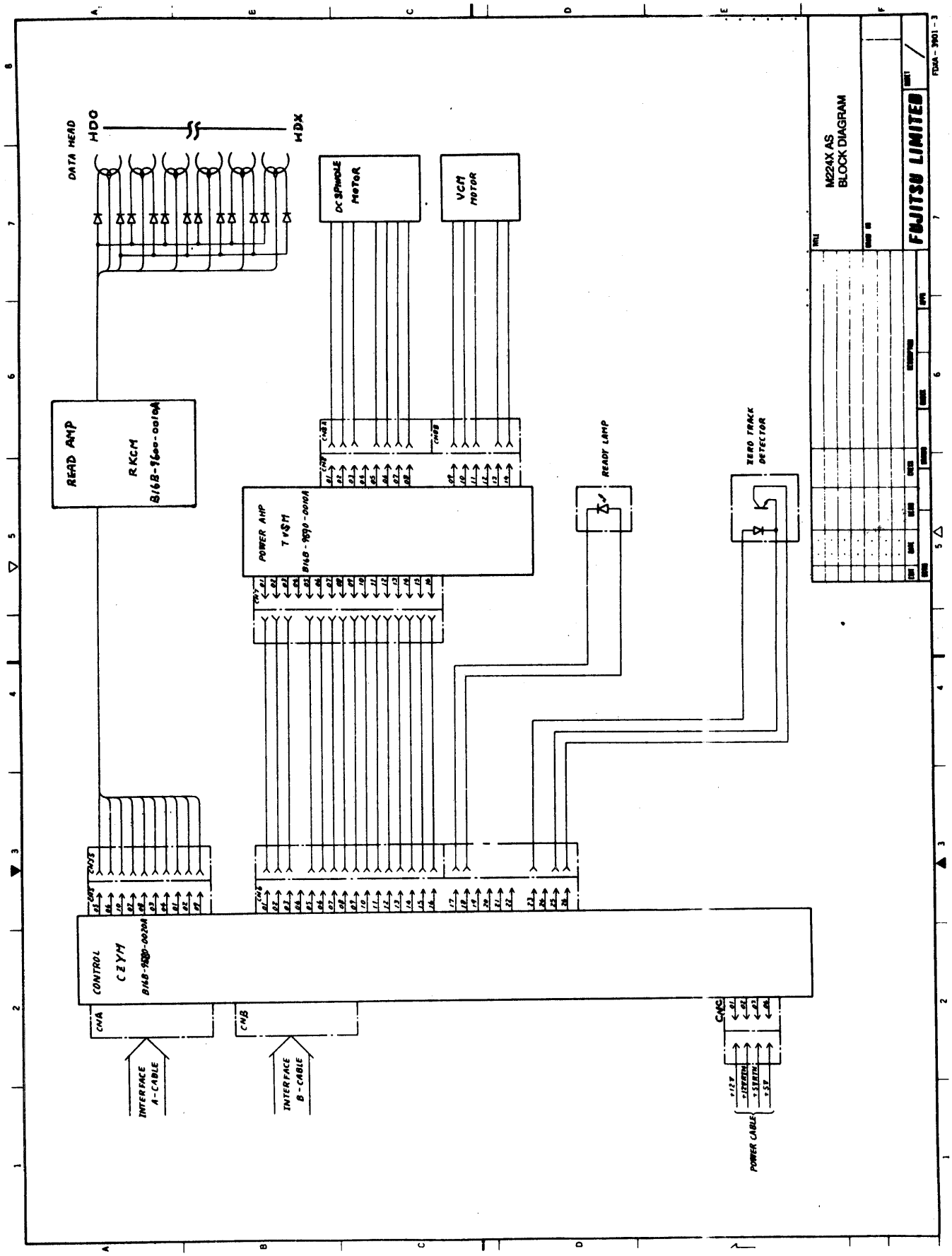


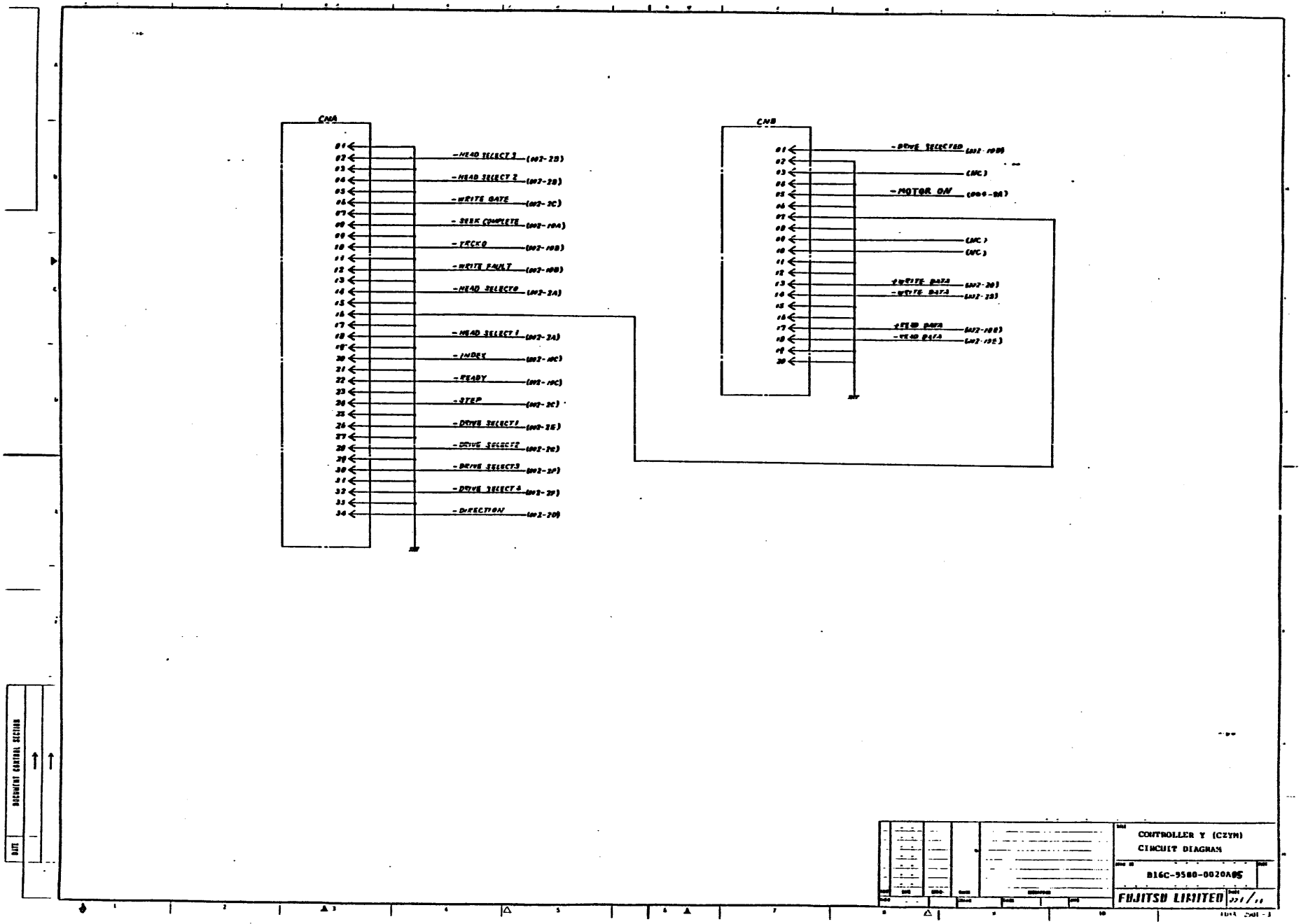
T ≤ 8μs

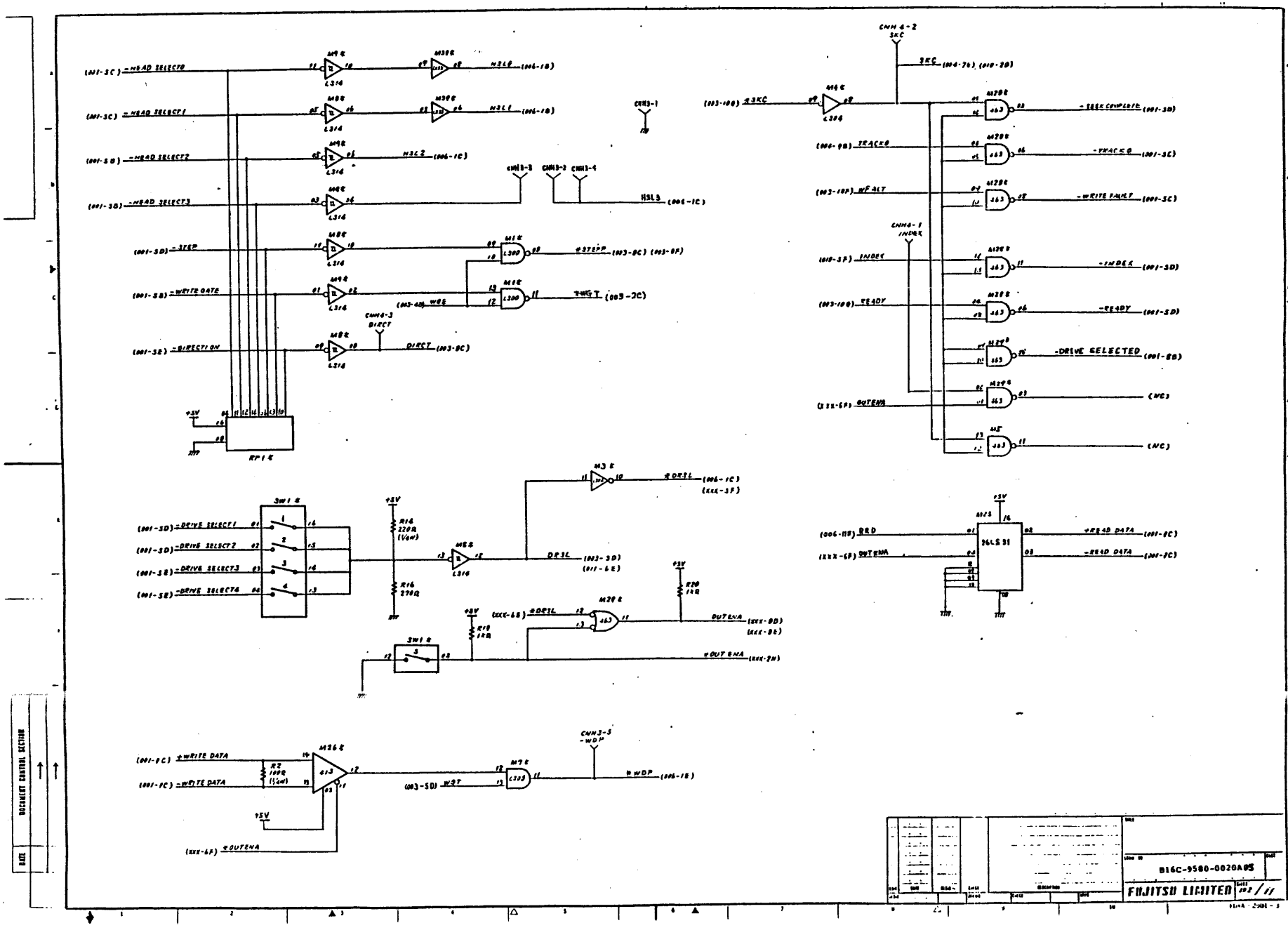
CHAPTER 6
SPARE PARTS

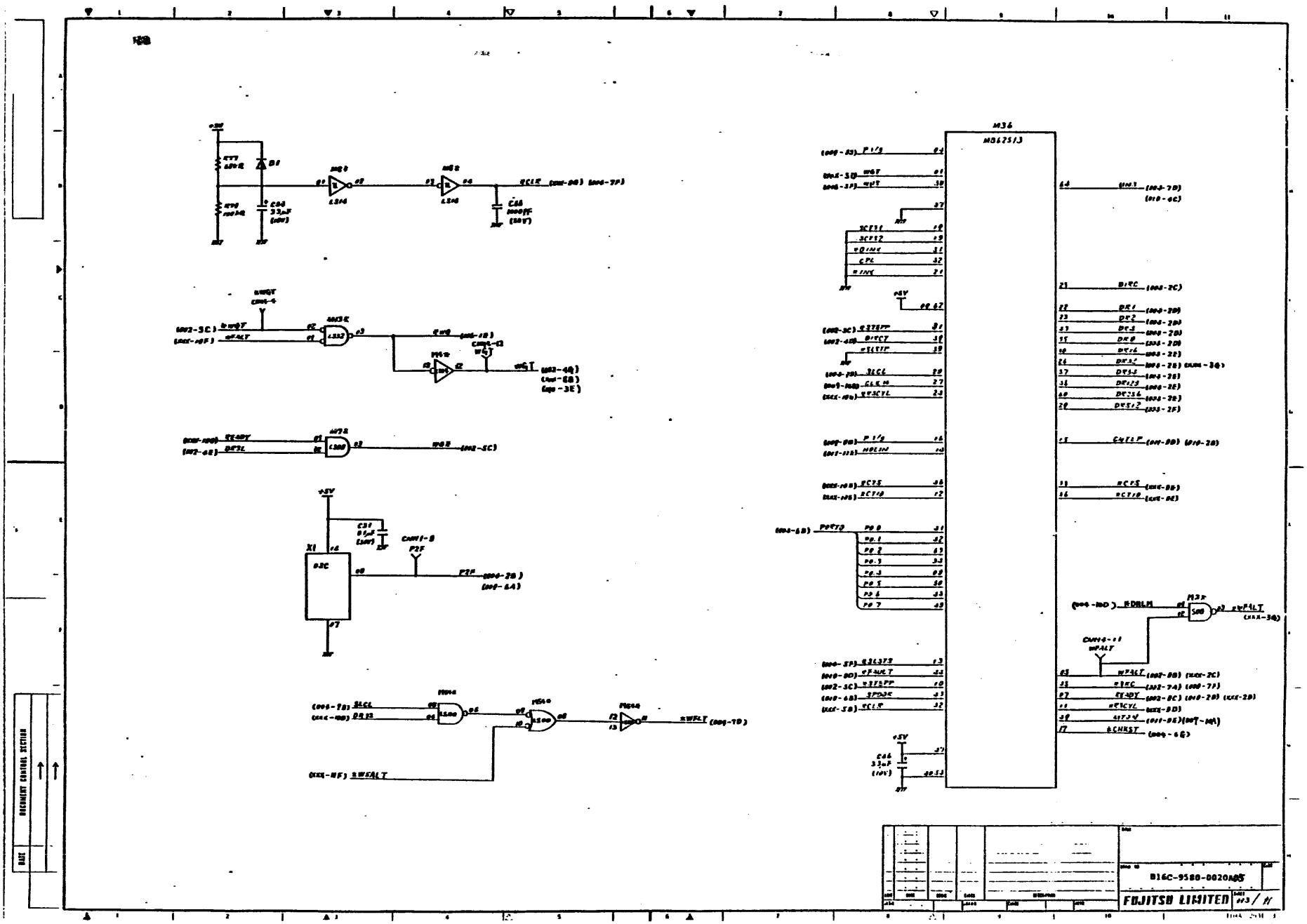
Item	Part Name	Part Number
1	DE (HDA)	
2	Control Y (CZYM)	B16B-9580-0020A
3	Power Amp S (TVSM)	B16B-9590-0010A
4	Read Amp C (RKCM)	B16B-9600-0010A
5	Terminator RM37	C76L-0970-0001
6	Front Panel (BEZEL)	B030-4800-X141A
7	Bracket, Right	B030-4800-X013A
8	Bracket, Left	B030-4800-X014A
9	Screws	F6-SBD-3 x 6 S (3mm x 6mm)

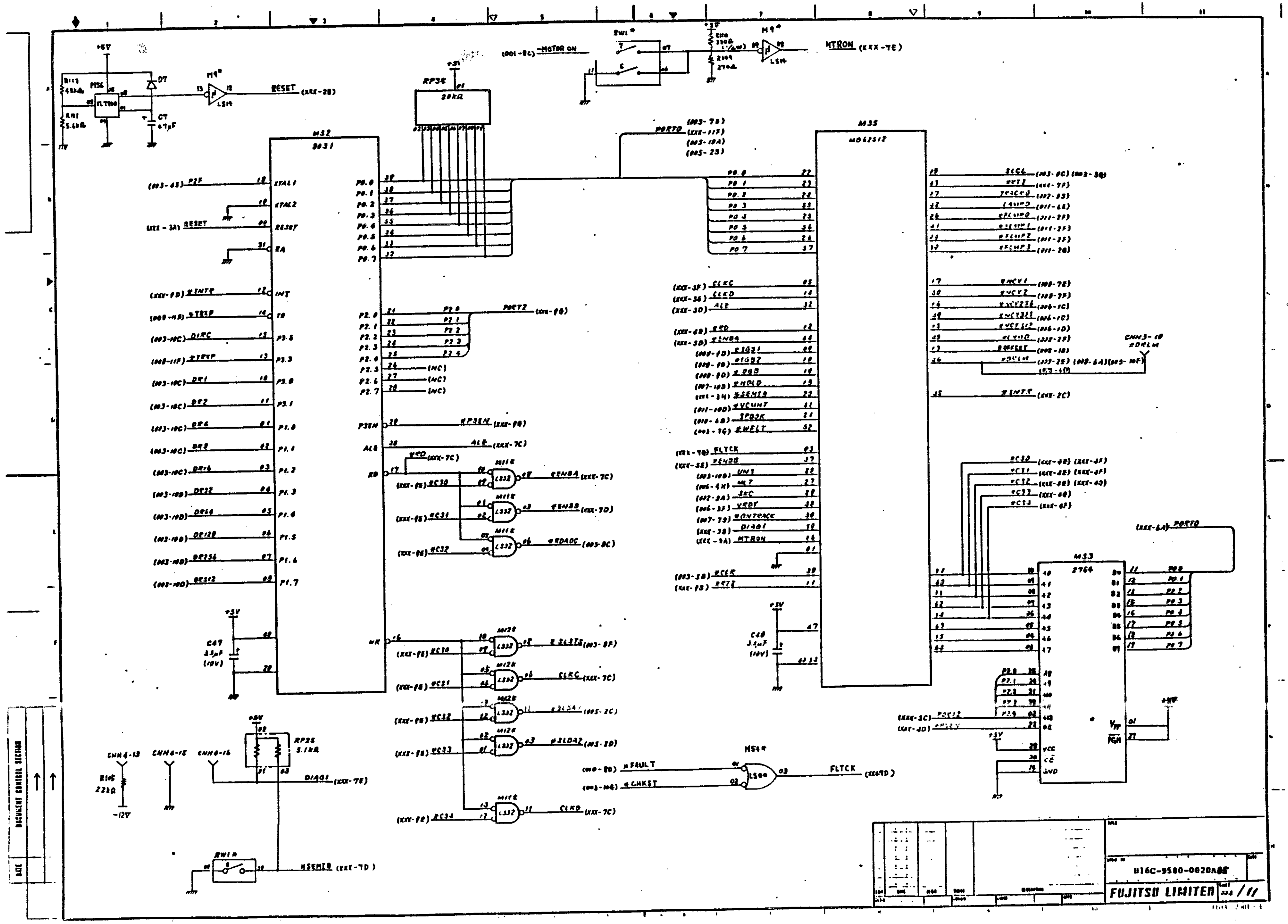
CHAPTER 7
SCHEMATIC




CNA
01
02
03
04
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
-HEAD SELECT 3 (U02-2B)
-HEAD SELECT 2 (U07-2B)
-WRITE GATE (U02-2C)
-SEEK COMPLETE (U02-10A)
-TRK0 (U02-10B)
-WRITE FAULT (U02-10B)
-HEAD SELECT0 (U02-2A)
-HEAD SELECT 1 (U02-2A)
-INDEX (U02-10C)
-READY (U02-10C)
-STEP (U02-2C)
-DRIVE SELECT1 (U02-2E)
-DRIVE SELECT2 (U02-2E)
-DRIVE SELECT3 (U02-2F)
-DRIVE SELECT 4 (U02-2F)
-DIRECTION (U02-20B)
CNB
01
02
03
04
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
-DRIVE SELECTED (U02-10B)
(NC)
-MOTOR ON (U04-8A)
(NC)
(NC)
+WRITE DATA (U02-20)
-WRITE DATA (U02-20)
+READ DATA (U02-10E)
-READ DATA (U02-10E)
CONTROLLER Y (CZYM)
CIRCUIT DIAGRAM
B16C-9580-0020A05
FUJITSU LIMITED

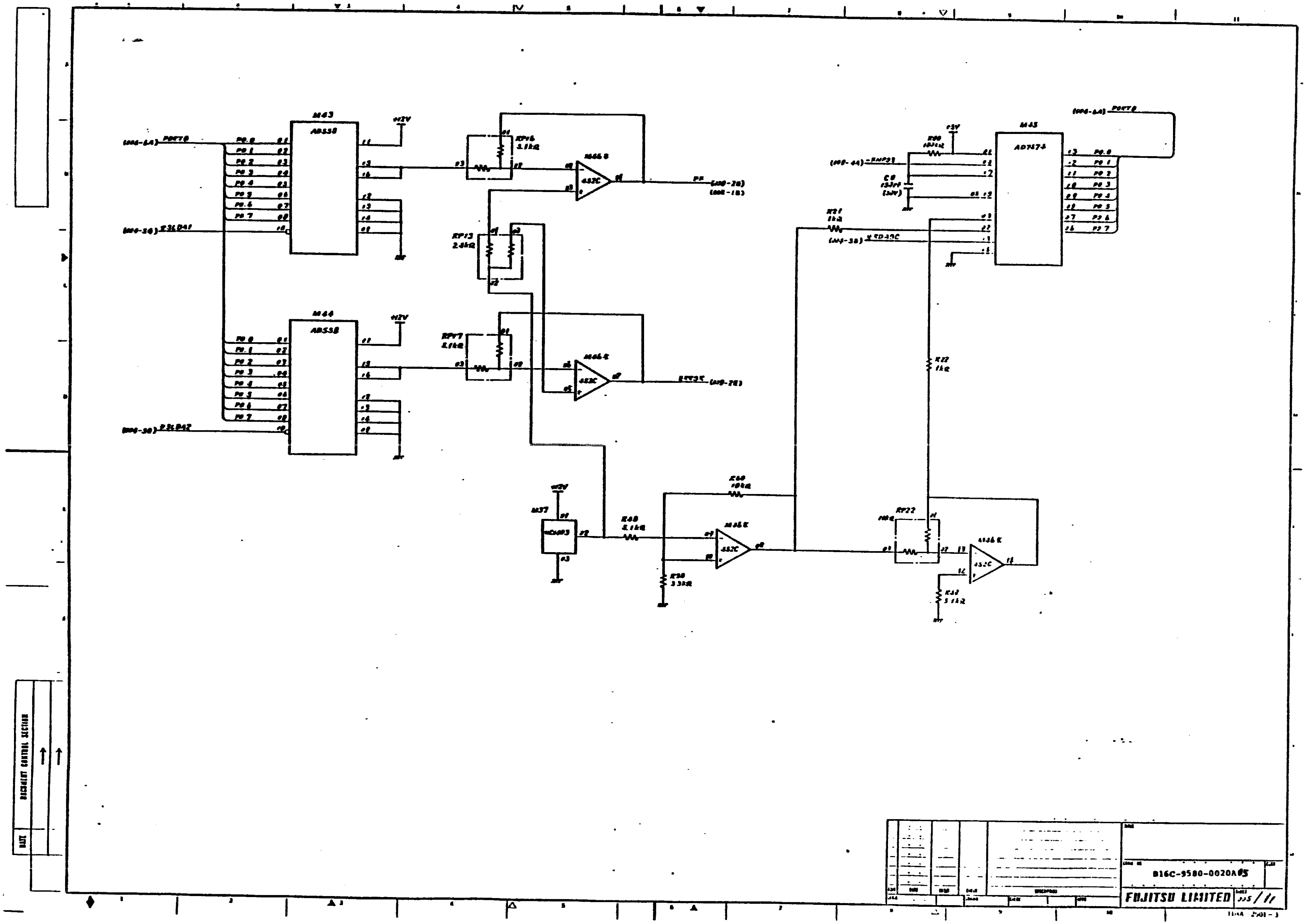

-HEAD SELECT0
-HEAD SELECT1
-HEAD SELECT2
-HEAD SELECT3
-STEP
-WRITE GATE
-DIRECTION
-DRIVE SELECT1
-DRIVE SELECT2
-DRIVE SELECT3
-DRIVE SELECT4
+WRITE DATA
-WRITE DATA
-SEEK COMPLETE
-TRACK 0
-WRITE FAULT
-INDEX
-READY
-DRIVE SELECTED
+READ DATA
-READ DATA
FUJITSU LIMITED
B16C-9580-0020A05

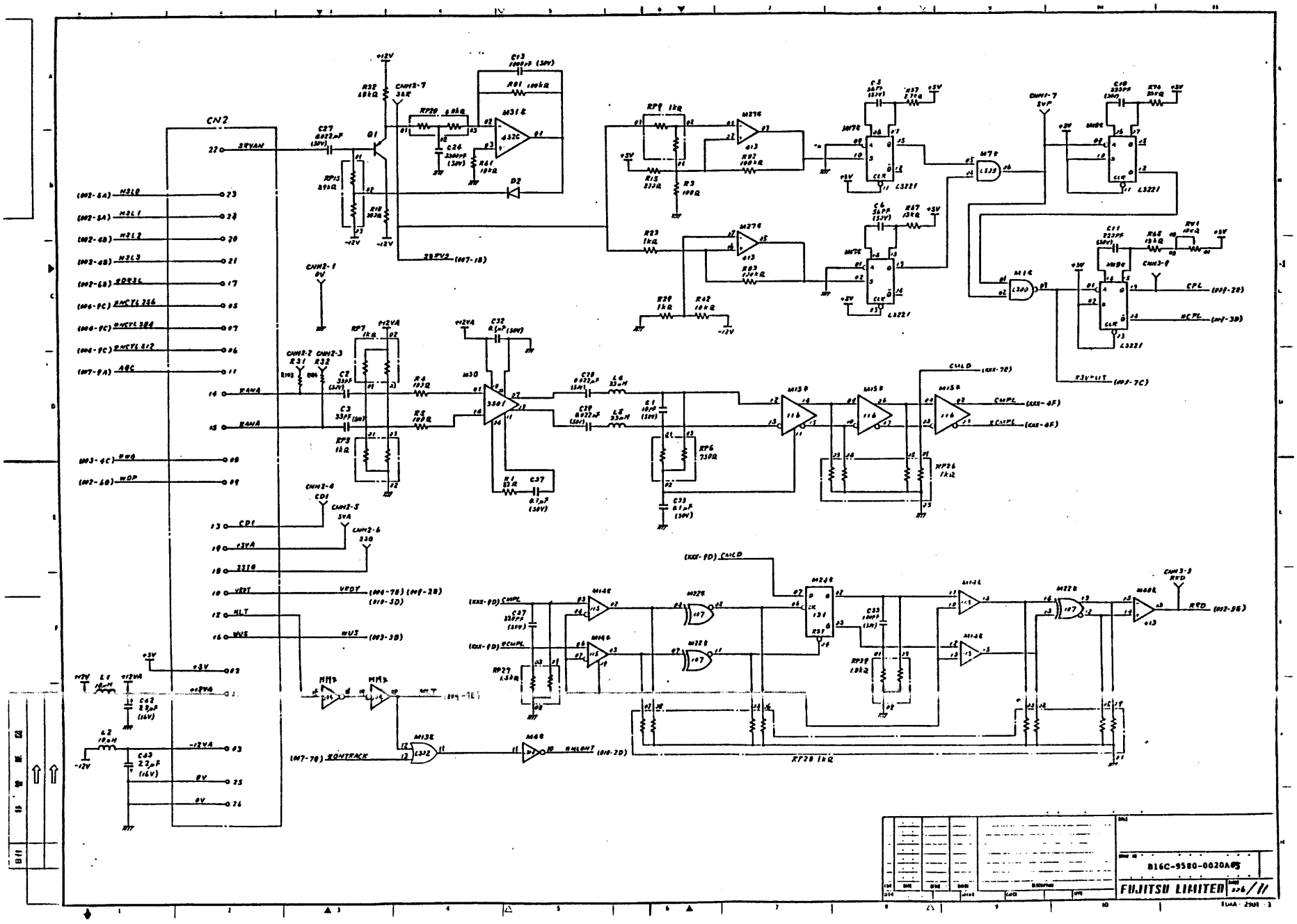

M36
MB62513
FUJITSU LIMITED
B16C-9580-0020A05

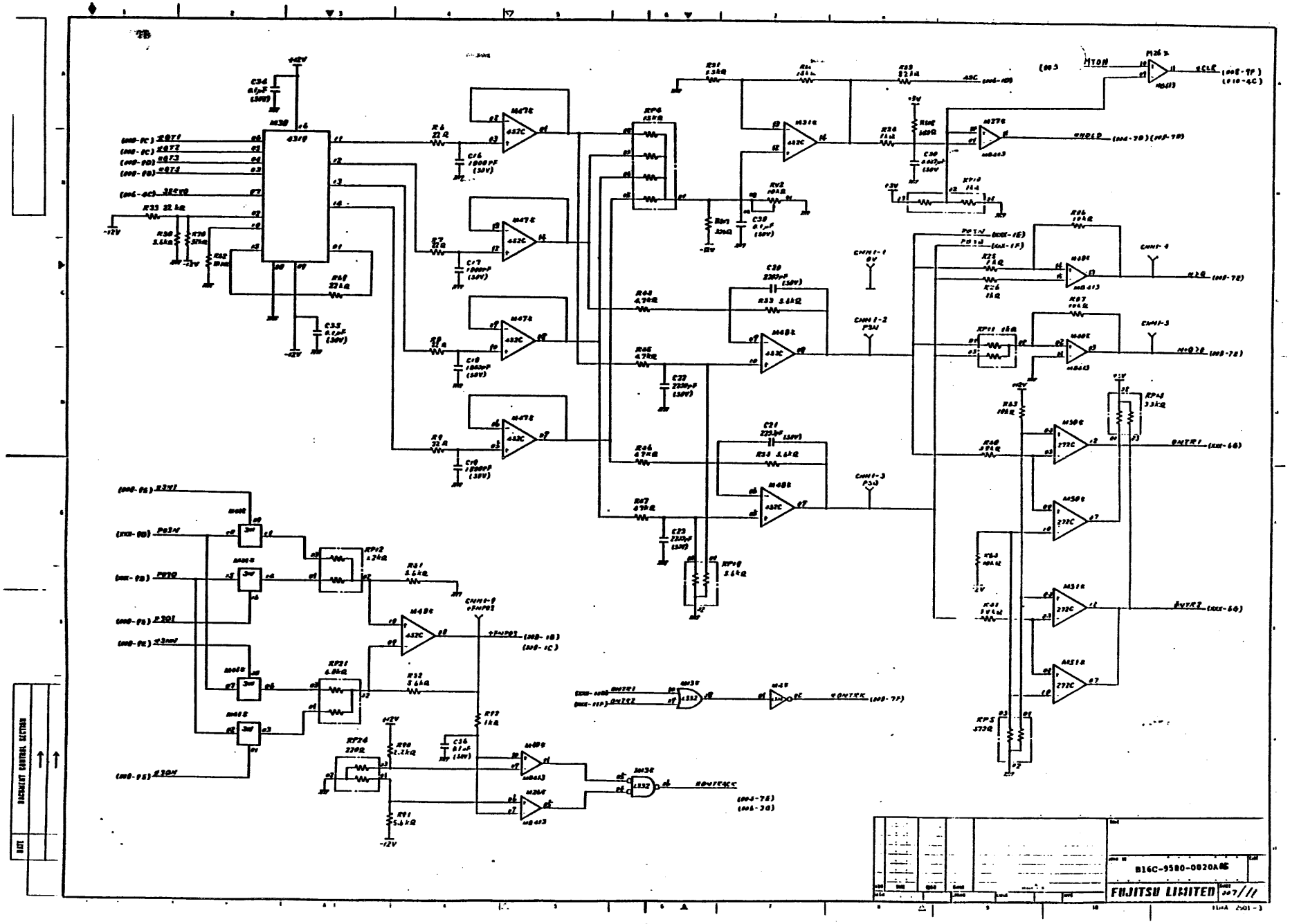


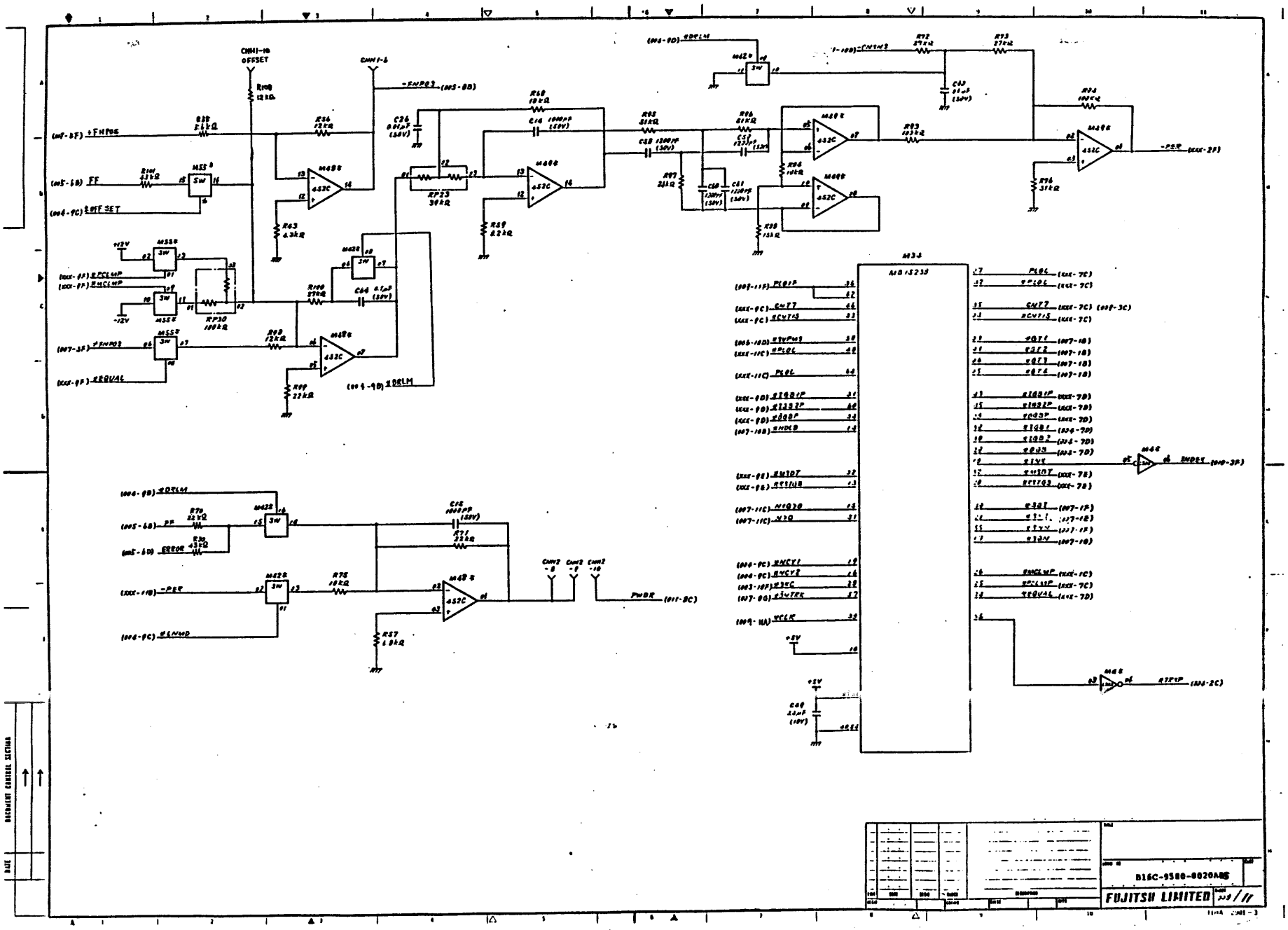
B03P-4805-0008A. . .01B

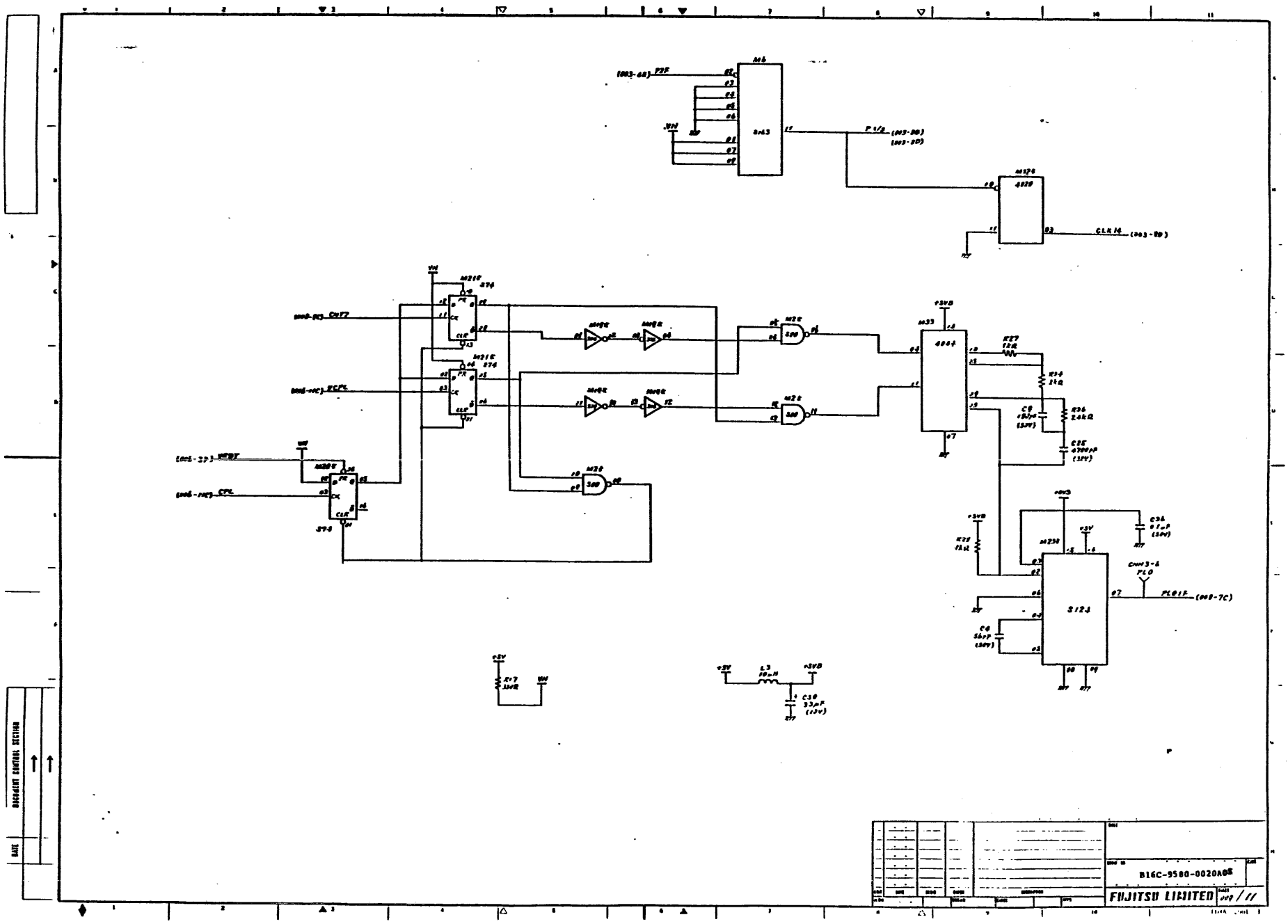
B03P-4805-0008A. . .01B

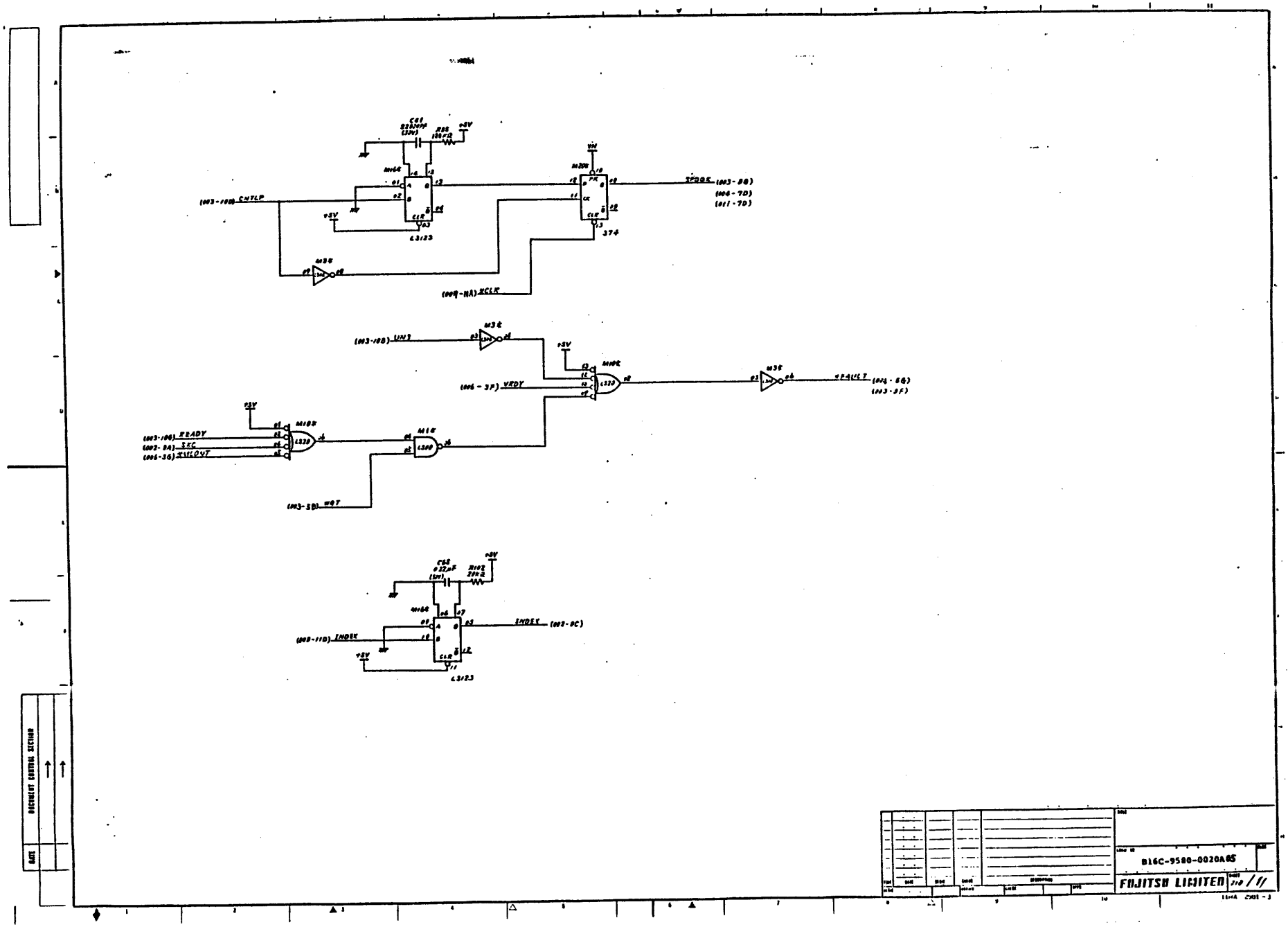


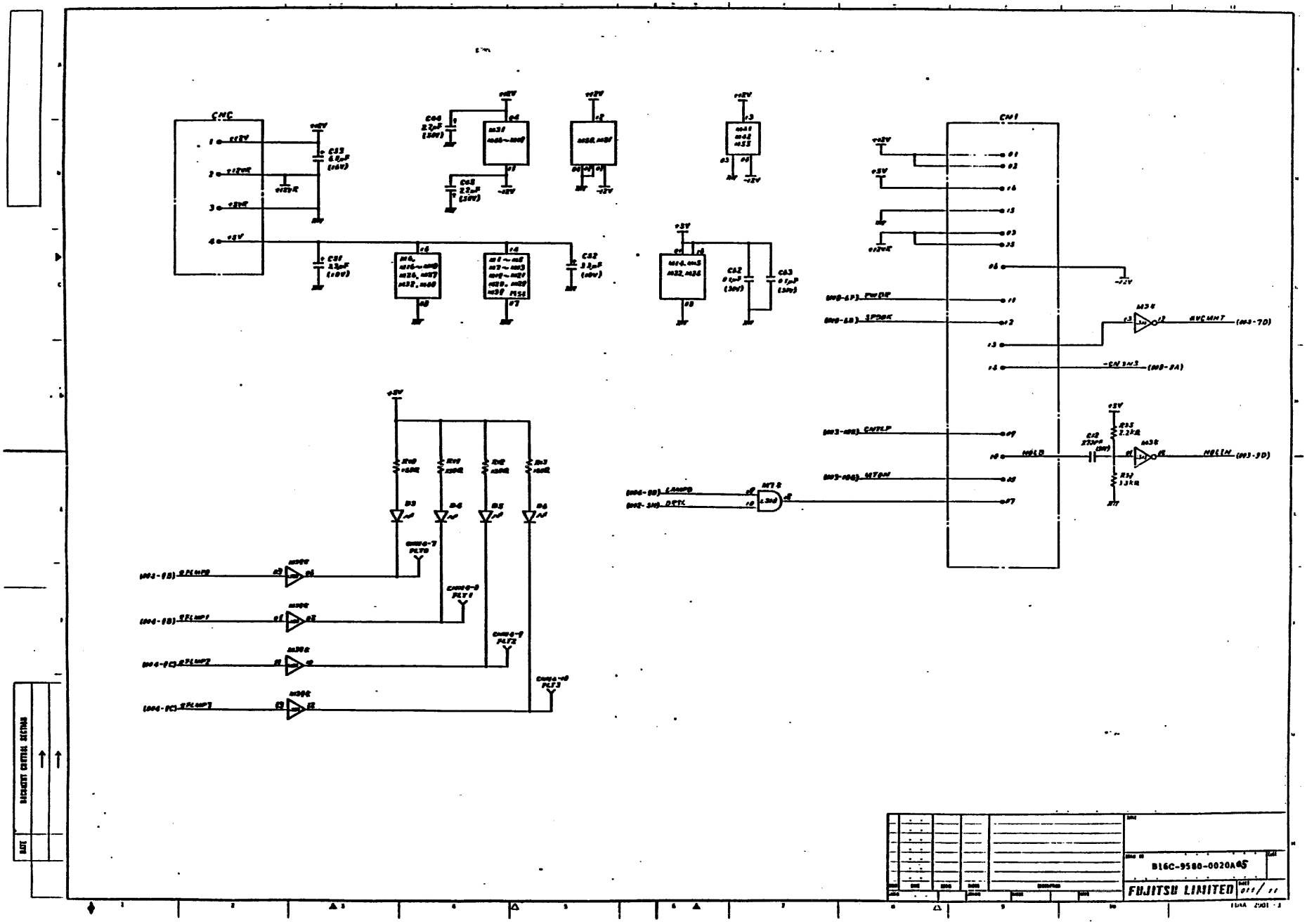

CN2
B16C-9580-0020A
FUJITSU LIMITED

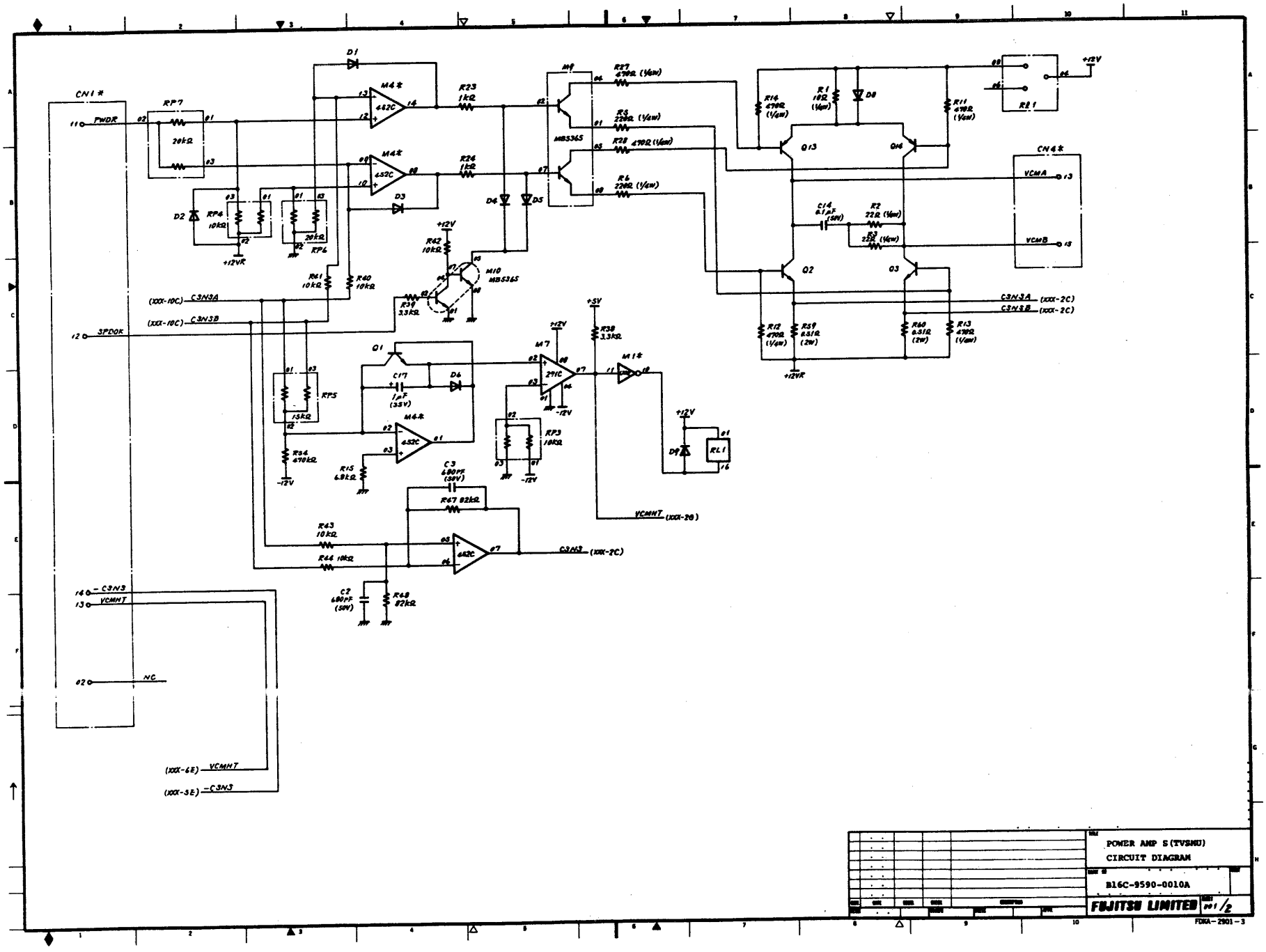

B16C-9580-0020A05
FUJITSU LIMITED

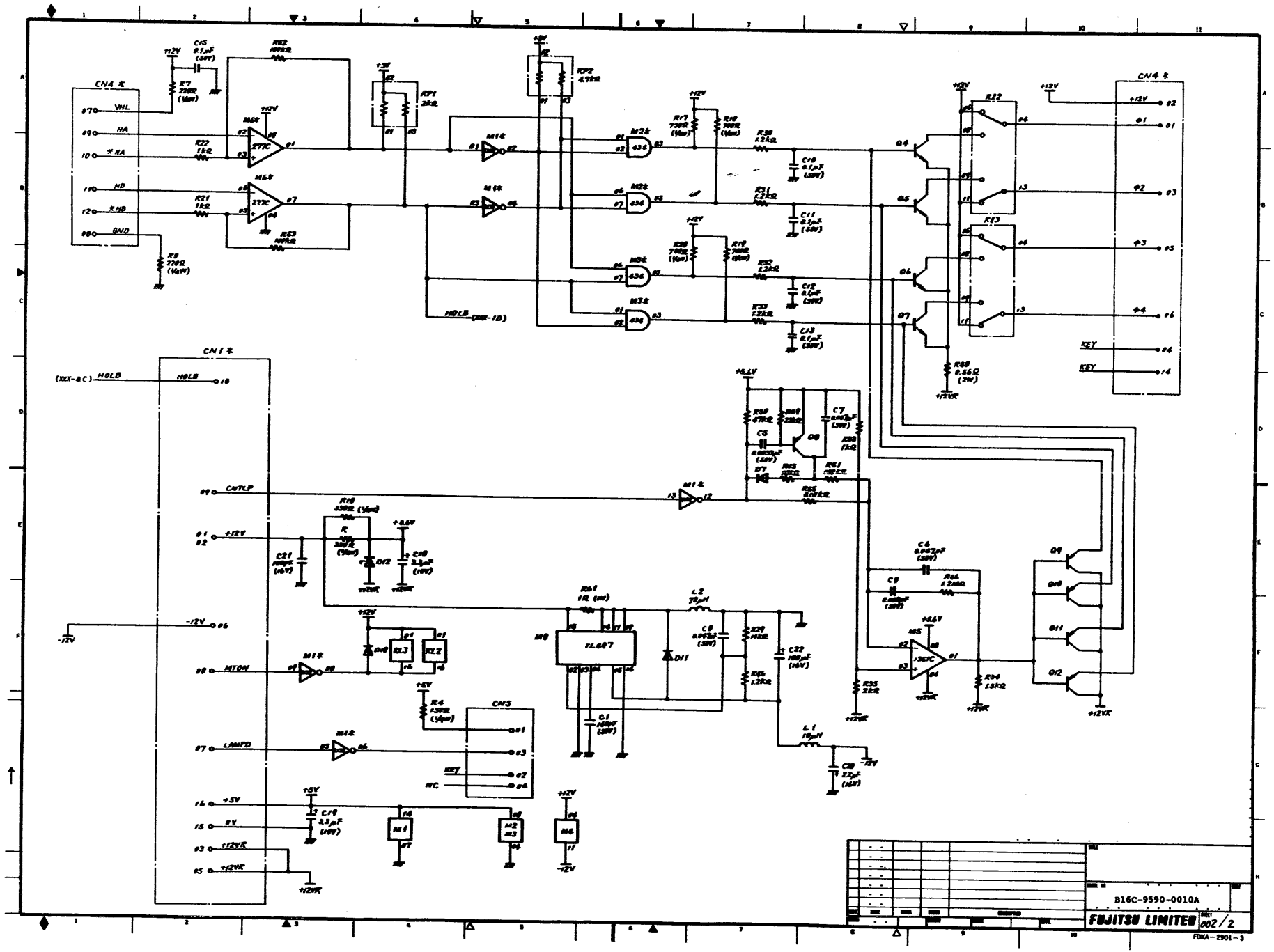

CH#1-16 OFFSET
CH#1-4
R100 12 kΩ
-FHP03 (005-8D)
(007-1F) +FHP06
(005-1B) FF
(004-9C) 2 OFF SET
R36 12kΩ
R43 4.3kΩ
C26 0.01μF (50V)
RP23 30kΩ
R58 10kΩ
C16 1000PF (50V)
C58 1500PF (50V)
R59 8.2kΩ
R95 22kΩ
R97 22kΩ
C60 1500PF (50V)
C61 1500PF (50V)
R94 100Ω
R98 150Ω
R96 61kΩ
C51 0.022μF (50V)
R93 10kΩ
R92 27kΩ
R91 27kΩ
C43 0.1μF (50V)
R95 100kΩ
R96 31kΩ
-PDR (006-2F)
+12V
-12V
(006-1F) RPCLMP
(006-1F) RHCLMP
R100 270kΩ
C64 0.1μF (50V)
RP30 100kΩ
(007-3F) +FHP03
R98 12kΩ
R99 22kΩ
(004-9B) RDRLM
(004-9B) RDRLM
R70 22kΩ
R71 5kΩ
(005-6B) PR
(005-1D) EEROR
(006-1B) -PEF
R75 10kΩ
R57 8.2kΩ
(004-9C) RENMD
C18 1000PF (50V)
R77 22kΩ
CH#2 -8
CH#2 -9
CH#2 -10
PWDR (011-8C)
M33 MB15233
(009-11F) PLOIP
(006-9C) CNT7
(006-9C) SCNT15
(006-10D) RSWPW3
(006-11C) RPLOL
(006-11C) PLOL
(006-9D) RIQ8IP
(006-9D) RIQ2IP
(006-9D) RQQ3P
(006-10B) RMDE0
(006-9E) RWIDT
(006-9E) RCTIR
(007-11C) MIQ20
(007-11C) M20
(006-9C) RHCY1
(006-9C) RHCY2
(003-10F) R35C
(007-9D) RSWTPC
(009-11A) VCLK
+5V
+5V
C69 2.2μF (10V)
PLOL (006-7C)
CNT7 (006-7C) (009-3C)
SCNT15 (006-7C)
RIQ8IP (006-7D)
RIQ2IP (006-7D)
RQQ3P (006-7D)
RIQ81 (006-7D)
RIQ82 (006-7D)
RQQ3 (006-7D)
RIVC (006-7D)
RWIDT (006-7B)
RCTIR3 (006-7B)
RIQ21 (007-1F)
RIQ11 (007-1E)
RIVV (007-1F)
RIQ2V (007-1D)
RHCLMP (006-7C)
RPCLMP (006-7C)
REQUAL (006-7D)
RTFVP (006-2C)
B16C-9580-0020ABS
FUJITSU LIMITED
DOCUMENT CONTROL SECTION
DATE

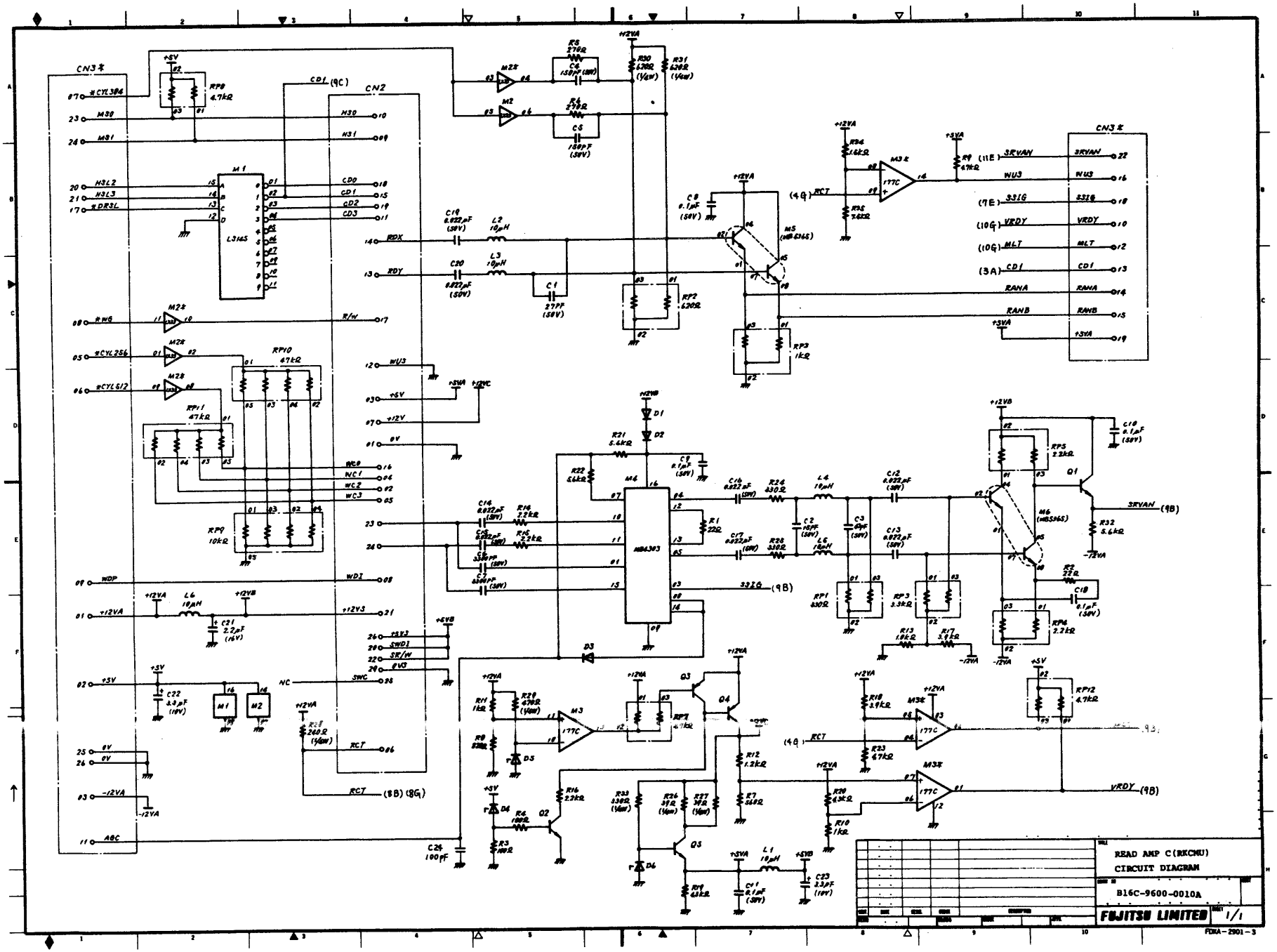



(003-10B) CNTLP
(009-11A) XCLR
SPDOK
(003-0B)
(006-7D)
(011-7D)
374
(003-10B) UNS
(006-3F) VRDY
FAULT
(004-66)
(003-3F)
(003-10B) READY
(002-8A) SEC
(006-3G) XVLDOUT
(003-3D) WGT
(009-11D) INDEX
INDEX (002-9C)
B16C-9580-0020A05
FUJITSU LIMITED


CN1C
CN1
B16C-9580-0020A
FUJITSU LIMITED


CN1*
PWDR
SPDOK
NC
-C3N3
VCMHT
(XXX-6E) VCMHT
(XXX-3E) -C3N3
RP7
20kΩ
M4*
4532C
D1
D2
D3
RP4
10kΩ
RP6
20kΩ
+12VR
R23 1kΩ
R24 1kΩ
M9
MBS365
R27 470Ω (1/4W)
R5 220Ω (1/4W)
R28 470Ω (1/4W)
R6 220Ω (1/4W)
D4
D5
+12V
R42 10kΩ
M10
MBS365
R39 3.3kΩ
R61 10kΩ
R40 10kΩ
(XXX-10C) C3N3A
(XXX-10C) C3N3B
Q1
C17 1μF (35V)
D6
RP5
15kΩ
R34 470kΩ
-12V
R15 6.8kΩ
M7
291C
M11*
+5V
R38 3.3kΩ
VCMHT (XXX-2B)
RP3 10kΩ
D9
RL1
C3 680PF (50V)
R67 82kΩ
R43 10kΩ
R44 10kΩ
C3A3 (XXX-2C)
C2 680PF (50V)
R68 82kΩ
R16 470Ω (1/4W)
R1 10Ω (1/4W)
D8
R11 470Ω (1/4W)
Q13
Q14
RE1
CN4*
VCMA
VCMB
C14 0.1μF (50V)
R2 22Ω (1/4W)
R3 22Ω (1/4W)
Q2
Q3
C3N3A (XXX-2C)
C3N3B (XXX-2C)
R12 470Ω (1/4W)
R59 0.51Ω (2W)
R60 0.51Ω (2W)
R13 470Ω (1/4W)
POWER AMP S(TVSMU)
CIRCUIT DIAGRAM
B16C-9590-0010A
FUJITSU LIMITED
001 1/2
FDKA-2901-3


CN4 A
CN1 A
CN5
HOLB
CNTLP
MTON
LAMPD
KEY
B16C-9590-0010A
FUJITSU LIMITED
002/2
FDXA-2901-3


READ AMP C(RKCNU)
CIRCUIT DIAGRAM
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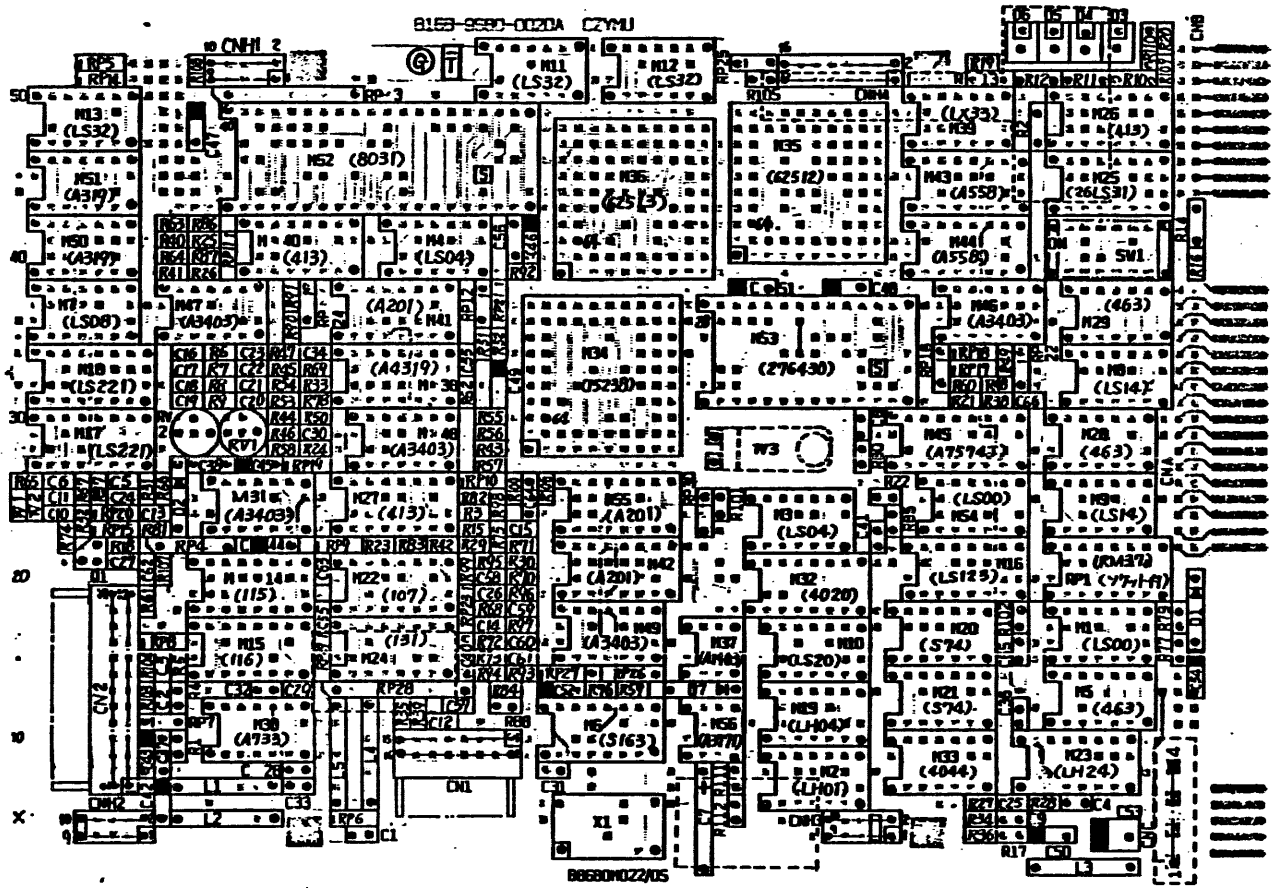
1/1
FORM-2901-3



CONTROLLER Y (C2YM)
MOUNTING DIAGRAM

B16D-9580-0020A05

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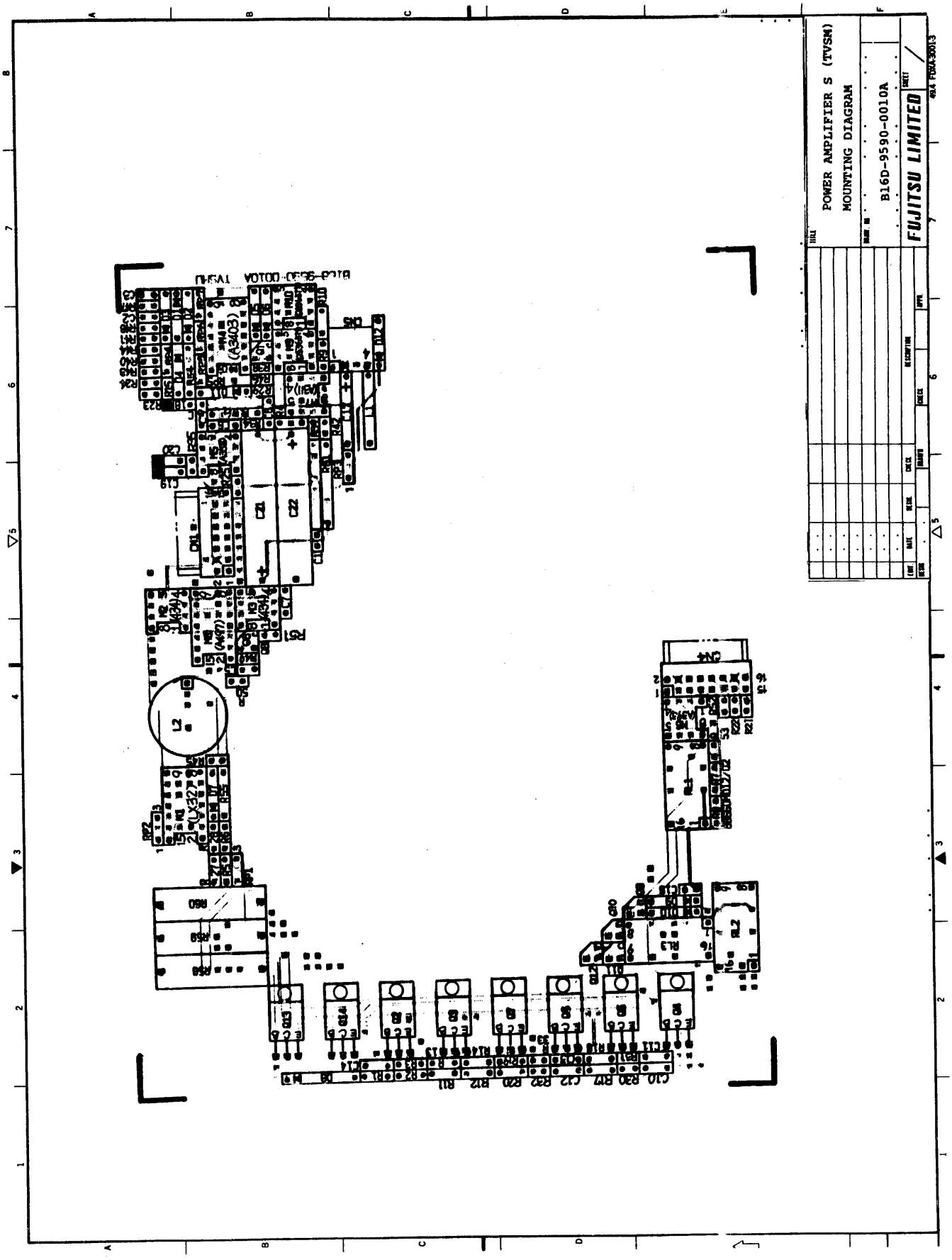
POWER AMPLIFIER S (TVSM)
MOUNTING DIAGRAM
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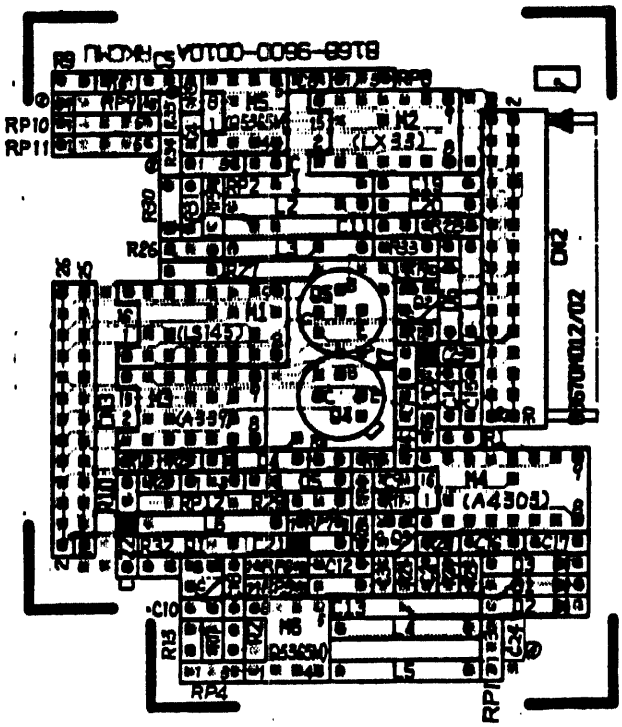

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